Errata

Title & Document Type: 3563A Control Systems Analyzer Service Manual - Volume II

Manual Part Number: 03563-90006

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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Agilent Technologies

Service Manual
HP 3563A
Control Systems Analyzer

Volume II

Serial Number
2927A00100

HEWLETT
PACKARD

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure the safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning **Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.**

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SAFETY SYMBOLS

General Definitions of Safety Symbols Used On Equipment or In Manuals.

⚠	Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.
ϟ	Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)
⏚ OR (⏚)	Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.
(⏚)	Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.
⏛ OR ⊥	Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.
∿	Alternating current (power line.)
⎓	Direct current (power line.)
≂	Alternating or direct current (power line.)

Warning **The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which if not correctly performed or adhered to, could result in injury or death to personnel.**

Caution The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

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Section VII
Fault Isolation

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Section VII: Fault Isolation

Section VII

Fault Isolation

Introduction

This section contains the information required to isolate failures to the circuit board level. To accomplish this, extensive use is made of the power-up tests and the self-tests. After isolating the failure to an assembly go to Section VIII, "Service" to continue the failure isolation process.

The fault isolation procedure assumes only one independent failure. Multiple failures may cause false results in the diagnostic tests.

Fault Isolation Procedures

Start Use table 7-1 to determine which troubleshooting procedure to begin with.

Table 7-1. Assembly Level Troubleshooting Guide

Symptom	Troubleshooting Procedure
Screen Blank Screen defective After power-on, > 3 min before keys active No response when key is pressed Incorrect response when key is pressed	"Initial Conditions Test" Section VII
"MONITOR TEST LOG" or "PROGRAM ROM DEAD" is displayed on power-up.	"Power-Up Tests" Section VII
Calibration fails Performance test fails	"Test All" Section VII
Digital Inputs fails	"Digital Input Failures" Section VII
Trigger fails	"Isolating Trigger Failures" Section VII
HP-IB fails	"A2, A22 System CPU/HP-IB" Section VIII
Intermittent failure	"Loop Mode and Intermittent Failures" Section VII

Reference For component locators and schematics refer to Section VIII.

For the location of cables and boards refer to figure 4-1 in Section IV.

To find a particular softkey refer to "**SPCL FCTN** Key Map".

To find the software revision code, refer to "Test Log and Fault Log Descriptions" in this section.

To understand the self-diagnostic process, refer to "Diagnostic Descriptions" in this section.

To understand the self-calibration process, refer to "Self-Calibration" in this section.

To understand the instrument's operation and signal mnemonics refer to Section VI.

Verify Use the oscilloscope waveforms in the "Waveforms" passage of this section to verify correct operation at various test points in the instrument.

Troubleshooting Hints

1. Intermittent cables can cause hardware failures.
2. Noise or spikes on power supplies can cause instrument failure.
3. Incorrect bias supply voltages can cause false diagnostic messages.
4. Use front panel diagnostics to isolate the problem before extensive troubleshooting.
5. It is possible that one circuit board can load another circuit board causing the wrong one to appear to be defective. This applies to both analog and digital signals.
6. Whenever possible, divide the circuit under test in half (half-splitting).
7. If the name of a nonnumerical key or "ENTRY Not Enabled" appears in the lower left of the display immediately after the power-up routine, there may be a stuck key or shorted trace on the keyboard (go to "A15 Keyboard" in Section VIII).
8. Do not remove any assembly from the instrument with the power on. There are several sensitive components in the instrument that may be damaged by power supply glitches.
9. To stop the instrument calibration, press softkey S8 (the last softkey) just after the display appears. Note: TEST ALL and SELF TEST may not be valid if this key is pressed before these tests are done.
10. A14 Mother Board failures are not isolated in this section. If the mother board is suspected of failing, refer to the "A14 Mother Board" discussion in Section VIII.
11. Measurements in this section are only approximate (usually ± 1 dB or 10%) unless stated otherwise.
12. The calibrator can be activated by performing the steps listed in the "Calibration Circuits Test" under "A30 Analog Source" in Section VIII. This allows the calibrator signals to be traced through the analog circuits. Using this technique, the calibrator can also be verified without the input assemblies.
13. If the instrument does not make a correct measurement but the self-tests pass, the instrument may need adjustment (refer to Section III).

Note

FFT Global Interface... FAILS
This failure message may occur if the instrument is internally set with unknown parameters before running the test (this can be caused by various measurement setups). Before running any of the FFT self-tests, press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

Recommended Test Equipment

The recommended test equipment for troubleshooting is listed in table 1-2. Any item which meets or exceeds the critical requirements can be substituted for the model listed. These procedures are designed to be run with a minimum amount of equipment.

Key Conventions

There are two types of keys on the HP 3563A, hardkeys and softkeys. Hardkeys are organized on the front panel according to functional group. See figure 7-1. In these procedures, the functional group is in brackets, the hardkeys appear in bold text, and the softkeys are in regular text.

1. For example: *Functional Group*

[Measurement] *Hardkey*
FREQ ...... FREQ
SPAN *Softkey*

[Entry]
1
0 ...... kHz

2. This example instructs you to first press the hardkey FREQ which is found in the Measurement group followed by the softkey FREQ SPAN. Next, enter the number 10 on the numeric keypad located in the Entry group. Specify the measurement unit by pressing the kHz softkey.

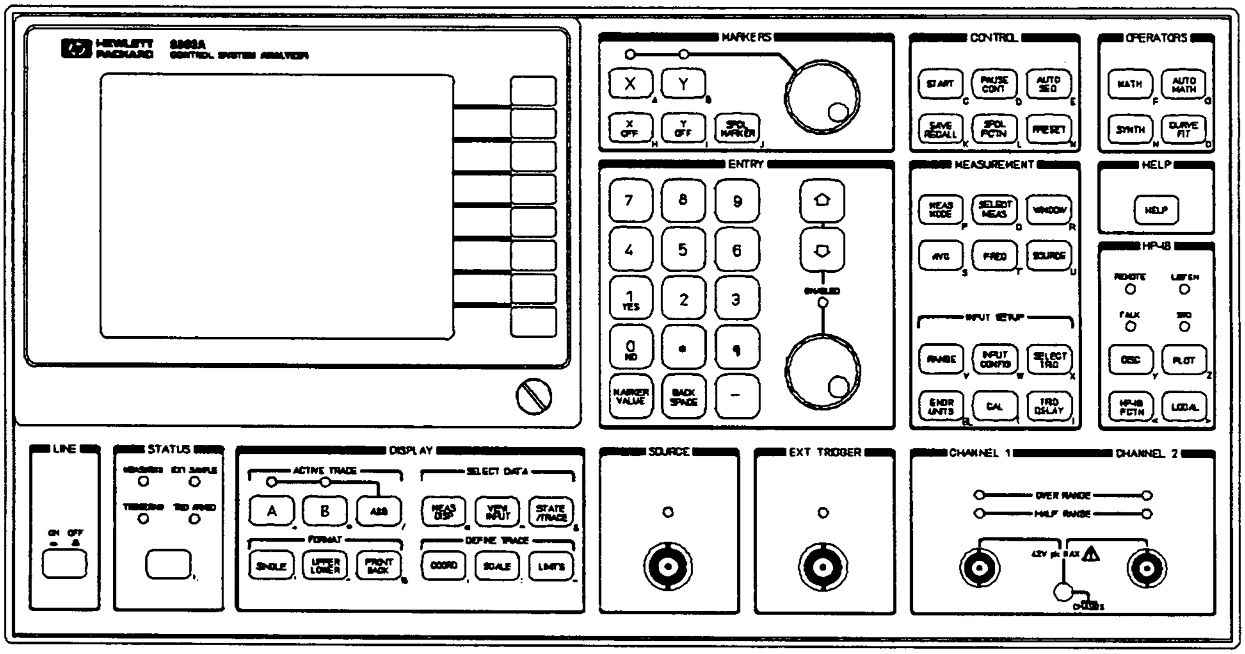


Figure 7-1 Front Panel Illustration

Logic Conventions

Positive logic convention is used in this manual unless otherwise noted. Positive logic conventions define a logic "1" or "High" as more positive voltage and a logic "0" or "Low" as the more negative voltage.

Safety Considerations

The HP 3563A is a Safety Class 1 instrument (provided with a protective earth terminal). The instrument and manuals should be reviewed for safety markings and instructions before operation. Refer to the safety symbol table in the preface of this manual.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A with the line power turned ON. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling and installing all parts to avoid unnecessary damage.

Warning

230 Vdc is present in the A18 power supply assembly even with the line switch in the OFF position and the power cord removed. Be extremely careful when working in the power supply area. This high voltage could cause serious personal injury if contacted. To discharge the capacitors holding this charge perform steps 1 through 3.

1. **Remove the power cord from the rear panel.**
2. **Remove the bottom cover and power supply shield.**
3. **Wait two minutes after turning the power off to allow the capacitors to discharge.**

Initial Conditions Test

The Initial Conditions Test is comprised of the following four procedures:

- Power Supply Check
- Keyboard Check
- Display Check
- Clock Check

Power Supply Check

1. Disconnect the power cord from the rear panel. Remove the bottom cover.
2. Connect the power cable and press the line switch ON.
3. Use table 7-2 to verify the power supply is operating correctly. If any of the values are incorrect start with the A18 Power Supply troubleshooting procedures in Section VIII.

Table 7-2. Power Supply Nominal Values
Return Location is A18TP13

Supply Name	Output Location	Nominal Voltage	Voltage Tolerance	Ripple Tolerance (P-P)
+5S	A14 J16-1	+5V	± 0.3V	50 mV
+30V	A14 W13-1	+30V	± 1.8V	10 mV
– 30V	A14 W13-2	– 30V	± 1.8V	10 mV
+15A	A14 W13-3	+15V	± 0.9V	10 mV
– 15A	A14 W13-4	– 15V	± 0.9V	10 mV
+5 FNTEND	A14 W13-5	+5V	± 0.3V	50 mV
+2.6V	A14 W13-6	+26V	± 0.16V	50 mV
+8S1	A14 W13-7	+8V	± 0.48V	25 mV
+8S2	A14 W13-8	+8V	± 0.48V	25 mV
+15S	A14 W13-9	+15V	± 0.9V	25 mV
– 15S	A14 W13-10	– 15V	± 0.9V	25 mV
OTEMPL	A14 W13-12	—	TTL Level High	—
PWRDNL	A14 W13-13	—	TTL Level High	—
PWRUP	A14 W13-14	—	TTL Level High	—

Keyboard Check

1. Press the line switch OFF.
2. Disconnect cable W10 (A14 J15) from the A14 Mother Board.
3. Connect the power cable and press the line switch ON.
4. Reset the keyboard by putting A15 J9 to the test (T) position, then back to the normal (N) position (see note).

Note

On some A15 revisions the A15 J9 jumper is not in a convenient location. If this is the case, the keyboard can still be reset using the following procedure:

a. Press the line switch OFF.
b. Disconnect cable W17 (A14 J16) from the A14 Mother Board.
c. Connect a +5V dc power supply and ground to W17, +5V to the red wire and ground to the black wire.
d. To reset the keyboard, cycle the +5V power supply off, then on.

---

5. The keyboard should respond as follows when it is reset:

   a. Beeps the beeper and flashes all the LEDs three times except CR12 (Triggering), CR17 (Half Range), and CR19 (Half Range). These LEDs will flash on and stay on since they are controlled by other assemblies.

   b. Beeps the beeper and then lights the LEDs one at a time in a pattern from left to right, top to bottom.

   c. Beeps the beeper again and then all the lights should remain on.

   d. RPG knobs can be check by rotating them clockwise or counter clockwise while watching the front panel. Remote, Listen, Talk, and SRQ LEDS flash in a clockwise or counter clockwise motion.

6. If the keyboard does not pass this test start with the A15 Keyboard troubleshooting procedures in Section VIII.
7. This test only validates part of the keyboard, it does not validate the system bus interface circuits.
8. Press the line switch OFF.
9. Connect cables W10 and W17 to the A14 Mother Board.

Note The keyboard cable (W10) can easily be connected wrong! After connecting the cable, verify that both rows of pins are connected. Red line on the cable goes to number one pin on connector

---

Display Check

1. Remove the top cover and press the line switch ON.
2. Set jumper A17 W1 (located in hole in display shield) to the test (T) position with the power on.
3. The pattern displayed should be the same as shown in figure 7-2. The main lines should all connect as shown and the lines in the lower right corner should be parallel.
   If this pattern is not displayed start with the Display Unit troubleshooting procedures in Section VIII.
4. Set jumper A17 W1 to the normal (N) position.

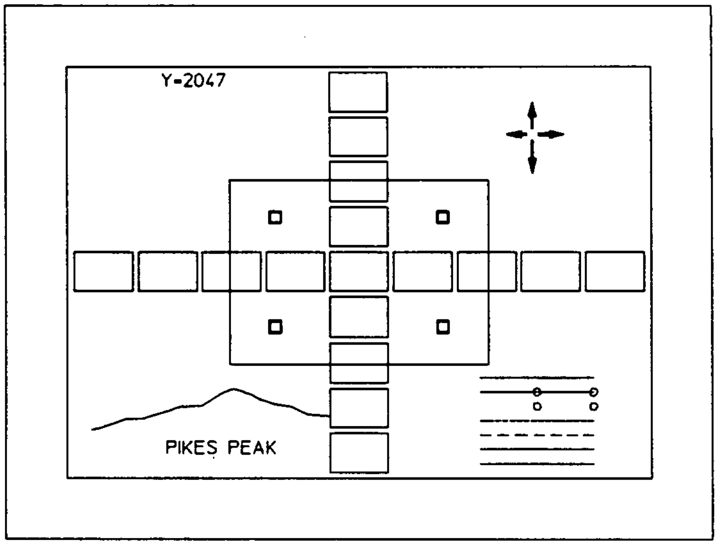


Figure 7-2. Display of Verification Pattern

Clock Check

1. Remove the top cover and press the line switch ON.
2. Use table 7-3 to verify various clocks in the instrument. If any of the values are incorrect, go to the troubleshooting procedures in Section VIII for the assemblies specified as the probable cause of failure.

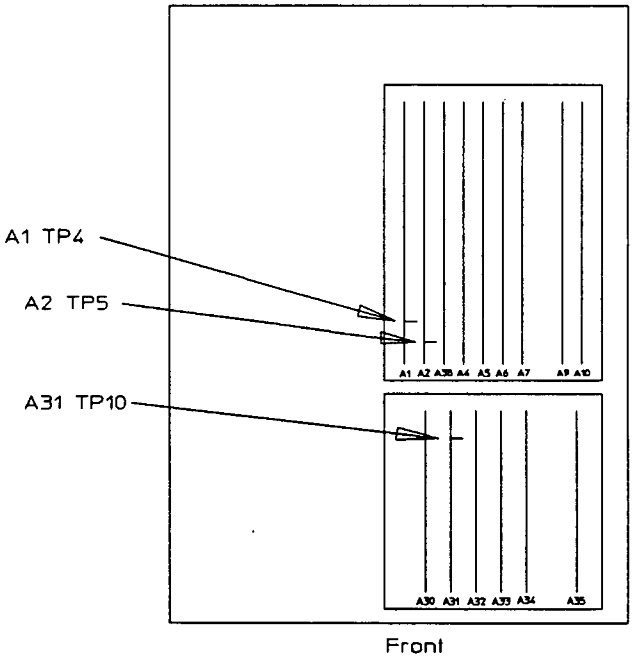


Figure 7-3. HP 3563A Top View, Cover Removed

Table 7-3. Clocks

Test Location*	Signal Name	Waveform #	Probable Cause	Go To
A31 TP10	20.48 MHz	#1	A31 Trigger	A31 Trigger Section VIII
A1 TP4	10.24 MHz	#2	A31 Trigger	A31 Trigger Section VIII
A2 TP5	8 MHz	#3	A2 System CPU	A2, A22 System CPU/HP-IB Section VIII

*Refer to figure 7-3.

If the fault has not been found, go to the following section, “Power-Up Tests”.

Power-Up Tests

The power-up test procedure is used when there is no display, incorrect display, or the instrument does not respond when a key is pressed. The "Initial Conditions Test" described in the preceeding pages, should be completed before performing the power-up test procedures.

The power-up tests consist of two sets of tests, low-level and high-level. The low-level tests exercise the A2 System CPU, the A38 Memory (Program ROM/Global RAM), the global bus, and the system bus. Fault and pass codes for these core assemblies are displayed using the A2 System CPU test LEDs (A2 DS3, A2 DS4). The high-level power-up tests exercise the A9 FFT, A7 FPP, A5 DGTL FLTR, and A6 D FLTR CONT assemblies. Faults on these assemblies are displayed in the test log (refer to table 7-8 for the description of these messages). The instrument performs a calibration if the power-up tests pass.

Power-up test failures may be caused by one of the following conditions:

1. A core assembly is defective (A2, A38).
2. An assembly on the system bus or global bus is defective, causing a bus failure.
3. The A15 Keyboard system bus interface circuits are defective. (This may be the case when the display is normal after power-up but the instrument does not respond when a key is pressed.)
4. A control line is defective.

Power-Up Test Procedure ONE

To find the cause of the failure, start by referring to the Power-Up Test Codes Table, table 7-6, for the location of the A2 Test LEDs and the LEDs to Hex code translation.

To verify the core assemblies are operating correctly, perform the following:

1. Remove the top cover.
2. Press the line switch ON.
3. Press the reset switch A2 S1 (reset switch on A2 CPU).
4. After the reset switch is pressed, the A2 System CPU should flash the test LEDs (A2 DS3, A2 DS4), light the LEDs one at a time, and cycle through several codes as listed in table 7-4. When finished, A2 DS1 should be off.

Table 7-4. LEDs Pass Sequence

Binary	Hex	Time Visible	Description
0000 0101	05	1s	System Processor test
0001 1110	1E	2.5s	Starting Program ROM check sum
1011 0101	B5	3.6s	Starting Global RAM Test
1011 0110	B6	15s	Starting high-level power-up test
1011 0111	B7	Remains Lit	Power-up Tests finished

5. Use table 7-5 to help isolate the cause of the failure. Start with the first line.

Table 7-5. Power-Up Self-Tests

LED Response	Description and What to do Next
LEDs pass sequence occurs but screen is defective. The System CPU and system bus are probably okay. The Global bus may be causing the failure	Go to Power-Up Test Procedure TWO.
LEDs displays a pass/error code > 4 minutes.	Note HEX error code and then go to Power-Up Test Procedure THREE.
A2 DS1 is ON. *or* No response to key presses.	Go to Power-Up Test Procedure THREE.

Power-Up Test Procedure TWO

Perform this procedure if the display is defective, but the LEDs pass sequence occurs and the instrument responds when SPCL FCTN is pressed.

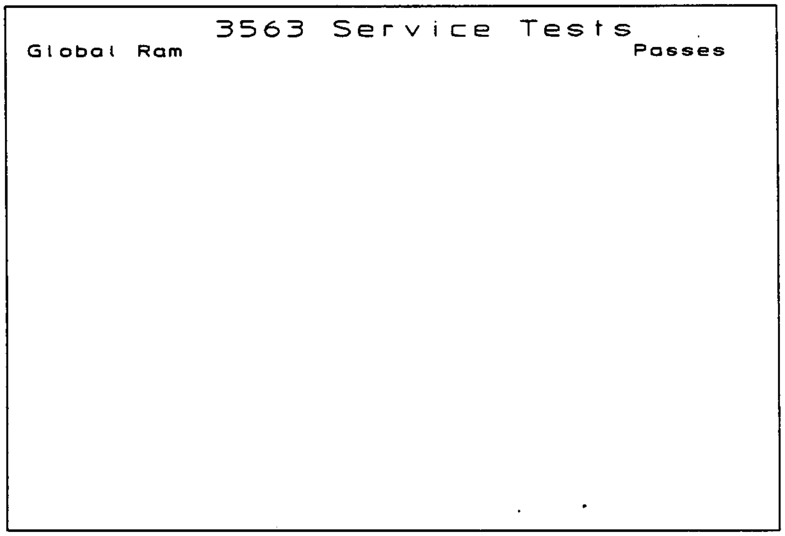
To find the cause of the failure, start by referring to the Power-Up Test Codes Table, table 7-6, for the location of the A2 Test LEDs and the LEDs to Hex code translation.

1. Press the line switch OFF.
2. Remove the following assemblies:
   A5 Digital Filter
   A7 FPP
   A9 FFT
3. Press the line switch ON and the HP 3563A keys as follows:

[Control]

SPCL FCTN ...... SERVIC TEST ...... TEST MEMORY ..... GLOBAL RAM

If the display does not appear as in figure 7-4, the A38 Memory board is probably the cause of the failure.



3563 Service Tests
Global Ram
Passes

Figure 7-4. Global RAM test passes

4. Press the line switch OFF.

5. Replace the A7 FPP assembly.

6. Press the line switch ON and the HP 3563A keys as follows:

┌ Control ┐

SPCL FCTN	......	SERVIC TEST	......	TEST PROC
	......	TEST FPP	......	FPP FUNCTION

If this test fails, the A7 FPP is probably the cause of the failure.

7. Press the line switch OFF.

8. Replace the A9 FFT assembly.

9. Press the line switch ON and the HP 3563A keys as follows:

┌ Control ┐

SPCL FCTN	......	SERVIC TEST	......	TEST PROC
	......	TEST FFT	......	FFT FUNCTION

If this test fails, start with the A9 FFT troubleshooting procedures in Section VIII.

10. Press the line switch OFF.
11. Replace the A5 DGTL FLTR assembly.
12. Press the line switch ON and the HP 3563A keys as follows:

⌈ Control ⌉
SPCL FCTN ...... SERVIC TEST ...... TEST PROC

...... TEST DFA ...... FILTER TEST

If this test fails, the A5 Digital Filter is probably the cause of the failure.

13. If the cause of the failure has not been found, go to “Control Line Tests”, which appears later in this section.

Power-Up Test Procedure THREE

Perform this procedure if the LEDs pass sequence does not occur, A2 DS1 is on, or the instrument does not display the special function menu when SPCL FCTN is pressed.

To find the cause of the failure, start by referring to the Power-up Test Codes Table, table 7-6, for the location of the A2 Test LEDs and the LEDs to Hex code translation.

1. If the A2 test LEDS display HEX IF (0001 1111), the battery may be failing. Verify A2 B1 measures ≅ 3.9V.
2. Press the line switch OFF.
3. Remove the bottom cover.
4. Disconnect cable W10 from the A14 Mother Board.
5. Remove the following assemblies:
    - A1 Digital Source
    - A4 Local Oscillator
    - A5 Digital Filter
    - A6 Digital Filter Controller
    - A9 FTT
    - A7 FPP
    - A10 Digital I/O
    - A38 Memory

Note

To remove the A10 Digital I/O board, side cover must be removed and cables to the A10 board must be disconnect.

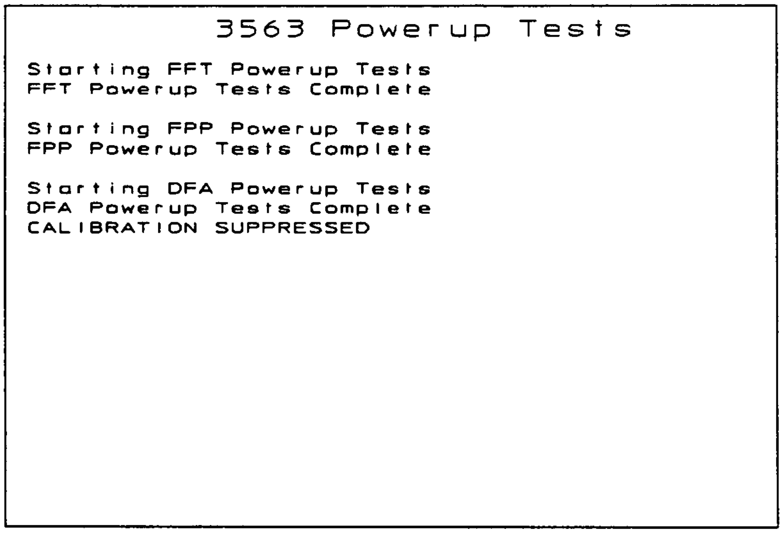
---

6. Pull the following assemblies up in their card nests so they are no longer connected to the A14 Mother Board:
    - A30 Analog Source
    - A31 Trigger
    - A32 ADC 1
    - A34 ADC 2

7. Press the line switch ON. The LEDs pass sequence should stop on Hex B1 (1011 0001) and A2 DS1 should be on. If Hex B1 is not displayed, start with the A2 System CPU troubleshooting procedures in Section VIII.
8. Press the line switch OFF.
9. Replace the A38 Memory assembly.
10. Press the line switch ON. The LEDs pass sequence should now occur, stopping on Hex B7 (1011 0111) and A2 DS1 should be off. Also, the display should appear as shown in figure 7-5.

Note The System CPU self-tests take up to 50 seconds to complete with several of the boards missing. Also, **SYSTEM FAULT** is displayed until all the boards are replaced.

The display flickers slighly when the boards are pulled out. If the display is defective or the LEDs pass sequence does not occur, the assembly failing is probably the A38 Memory Board (an A2 CPU global bus driver or the A17 Display Interface could be failing, but this is improbable).



```
              3563 Powerup Tests

Starting FFT Powerup Tests
FFT Powerup Tests Complete

Starting FPP Powerup Tests
FPP Powerup Tests Complete

Starting DFA Powerup Tests
DFA Powerup Tests Complete
CALIBRATION SUPPRESSED
```

Figure 7-5. Display Active

11. Press the line switch OFF.

12. Connect the A15 Keyboard cable (W10) to the A14 Mother board.

Note

The keyboard cable (W10) can easily be connected *wrong*! After connecting the cable, verify that both rows of pins are connected. Red line on the cable goes to number one pin on the connector.

---

13. Press the line switch ON. The LEDs pass sequence should occur, stopping on Hex B7 (1011 0111), and A2 DS1 should be off. The keys should now be active. If the LEDs pass sequence does not occur or the keys are not active, the probable cause of the failure is the A15 Keyboard system bus interface circuits. Refer to the A15 Keyboard troubleshooting procedures in Section VIII.

14. Replace the A1 Digital Source assembly as follows:

    a. Press the line switch OFF.

    b. Replace the assembly.

    c. Press the line switch ON.

    d. The LEDs pass sequence should occur, stopping on Hex B7 (1011 0111), and A2 DS1 should be off. If the LEDs pass sequence does not occur, the keys are not active, or the display is defective, the last board inserted is the probable cause of the failure.

15. Perform steps 14a through 14d for each of the remaining assemblies. Replace the assemblies in the following order:

    a. A9 FFT
    b. A6 Digital Filter Controller
    c. A7 FPP
    d. A4 Local Oscillator
    e. A31 Trigger
    f. A5 Digital Filter
    g. A10 Digital I/O
    h. A34 ADC 2
    i. A30 Analog Source
    j. A32 ADC 1

16. If the failure has not been isolated, use table 7-6, Power-Up Tests Code Table, and the Control Line Test to help isolate the failure.

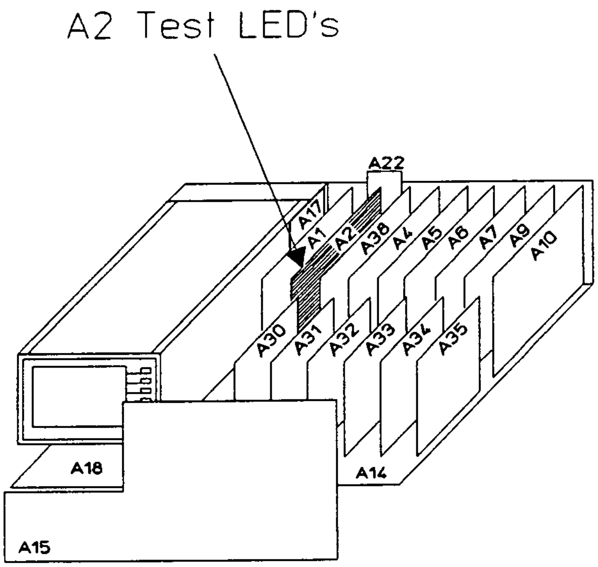
Power-Up Tests Code Table

After the power-up tests are completed, use table 7-6 to help determine the cause of the failure. (Refer to the beginning of this section for the description of the power-up test sequence). The table lists the tests in the order they are run. The A2 Test LEDs Hex code is listed on the vertical axis of the table. The assemblies and subblocks tested or used by the power-up tests are listed on the horizontal axis of the table.

There are two symbols used in the Power-Up Test Codes: **O** and a **filled box**. When the symbol "**O**" is used in the table, the assembly or subblock is used in the test but is not a likely cause of the failure. When the **filled box** is used in the table, the assembly or subblock is the probable cause of the failure. **No symbol** means the assembly or subblock is not used in the test.

Note

Shorts on the system bus, the global bus, an interrupt line, or the reset line, can cause false error codes. If an error code is caused by the last assembly inserted, it is probably the assembly defective.



Example:

LEDs	○○○●	●●●●
Binary	0001	1111
Hex	1	F
Chart Line	#21	

LED ON = 1
LED OFF = 0

Binary	**Hex**
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

Hex Error Code	**to Chart Line#**
01 to 04	2
05 to 06	3
07 to 0B	1
0C to 0F	6
10 to 1C	4
1D	1
1E	7
1F	21
20 to 33	12
34 to 3F	1
40 to 53	13
54 to 59	1
5A	9
5B	10
5C	11
5D to 5F	1
60 to 73	14
74 to 79	1
7A	10
7B	9
7C	11
7D to 7F	1
80	1
81	23
82	24
83	25
84 to 86	15
87	17
88	18
89	19
8A to 8C	16
8D	20
8E to 8F	1
90 to 9F	26
A0 to AF	27
B0	1
B1	8
B2 to B4	1
B5	22
B6	30
B7	31
B8 to BF	1
C0 to CF	5
D0 to DF	28
E0 to EF	29
F0 to FF	1

Table 7-6. Power-Up Test Codes

The filled box means the assembly or subblock is the most likely cause of the failure message.

The symbol O means the assembly or sublock is used in the circuit but is not the most likely cause of the failure message.

No symbol means the assembly or subblock is not used in the test.

Note: These tests are run in order starting with the monitor ROM test. The error code is for the first test that fails. A pass code indicates a failure on the next test.

Assembly/Subblock

Chart Line #	Hex Pass/Error Code	Test Description	8 MHz Clock	+5S	U100 System Processor	CPU Monitor ROM	CPU Monitor RAM	CPU Assembly	Mother Board	System Bus	Program ROM High	Program ROM Low	FFT System Interface	Global Bus. go to Power-Up Test #	Global RAM High	Global RAM Low
			A2	A18	A2	A2	A2	A2	A14	—	A38	A38	A9	—	A38	A38
System CPU Tests																
1	Undefined	Initial Power-Up	▨	O	▨	O	O	▨								
2	01 to 04	Monitor ROM	O	O	O	▨	O	O								
3	05 to 08	System Processor	O	O	▨	O	O	O								
4	10 to 1C	Monitor RAM Test Failure	O	O	O	O	▨	O								
5	C0 to CF	Monitor RAM Address Failure	O	O	O	O	▨	O								
6	0C to 0F	Timer and Interrupt Failures	O	O	O	O	O	▨								
Program ROM and System Bus Tests																
7	1E	Start Program ROM Check Sum	O	O	O	O	O	O	O	▨	▨	▨				
8	B1	Program ROM Installed ?	O	O	O	O	O	O	O	O	▨	▨				
9	5A,7A*	Program ROM Failure Low Byte	O	O	O	O	O	O	O	▨		▨				
10	5B,7B*	Program ROM Failure High Byte	O	O	O	O	O	O	O	▨	▨					
11	5C,7C*	Program ROM Failure, Both Bytes	O	O	O	O	O	O	O	▨	▨	▨				
12	20 to 33	Program ROM, Chip Failure, High Byte	O	O	O	O	O	O	O	O	▨					
13	40 to 53	Program ROM, Chip Failure, Low Byte	O	O	O	O	O	O	O	O		▨				
14	60 to 73	Program ROM, Chip Failure, Both Bytes	O	O	O	O	O	O	O	O	▨	▨				
15	84 to 86	Program ROM Failure, System Bus Good	O	O	O	O	O	O	O	O	▨	▨				
16	8A to 8C	Program ROM Failure, System Bus Good	O	O	O	O	O	O	O	O	▨	▨	O			
17	87	System Bus Failure, High Byte	O	O	O	O	O	O	O	▨	O	O				
18	88	System Bus Failure, Low Byte	O	O	O	O	O	O	O	▨	O	O				
19	89	System Bus Failure, Both Bytes	O	O	O	O	O	O	O	▨	O	O				
20	8D	No ROM Passes Check Sum, System Bus Good. Check System Address Bus	O	O	O	O	O	O	O	▨	▨	▨				
21	1F	Program ROM and System Bus Tests Pass	O	O	O	O	O	O	O	O	O	O				
Global Ram Test																
22	B5	Starting Global RAM Test	O	O	O	O	O	O	O	O	O	O		▨	O	O
23	81	Global RAM Failure, Both Bytes	O	O	O	O	O	O	O	O	O	O		O	▨	▨
24	82	Global RAM Failure, High Byte	O	O	O	O	O	O	O	O	O	O		O	▨	
25	83	Global RAM Failure, Low Byte	O	O	O	O	O	O	O	O	O	O		O		▨
26	90 to 9F	Global Bus Failure Bit, "N"	O	O	O	O	O	O	O	O	O	O		▨	O	O
27	A0 to AF	Global RAM Address Failure, Bit "N" Check Global Address Bus	O	O	O	O	O	O	O	O	O	O		▨	▨	▨
28	D0 to DF	Global RAM Failure, Bit "N"	O	O	O	O	O	O	O	O	O	O		O	▨	▨
29	E0 to EF	Global RAM Refresh Failure, Bit "N"	O	O	O	O	O	O	O	O	O	O		O	▨	▨
30	B6	Executing High Level Power-Up Tests	O	O	O	O	O	O	O	O	O	O	O	O	O	O
31	B7	Power-Up Tests Finished														

*No Information about System Bus

Test All

The Test All sequence thoroughly exercises the digital and the analog hardware in the instrument. This self-diagnostic actually does several types of measurements to determine what is operating correctly. When a fault is found the self-diagnostic exercises suspected circuits using digital signals generated internally, reading status registers, and using the internal analog source and calibrator. The Test All sequence then uses logic to determine the most likely failure based on the results of these measurements.

All failure messages are displayed in the Test Log. For a description of the Test Log messages, refer to "Test Log and Fault Log Descriptions" in this section. If the Test All sequence does not isolate the defective assembly, the individual self-tests for the suspected assemblies can be done individually to help isolate the failure. Use table 7-8, "Test All Messages" as a reference when running any of the service tests. When a test passes, the assemblies and subblocks exercised are most likely operating correctly.

The Test All feature does not isolate failures on the following assemblies:

Core Assemblies
A31 Trigger
A15 Keyboard
A18 Power Supply
A12 Mother Board
A17 Display Interface
HP Digital Display
System and global control lines

If a keyboard related problem is suspected, go to the A15 Keyboard troubleshooting procedures in Section VIII after performing the Test All procedures. If the instrument does not respond when a key is pressed or the display is defective, go to "Initial Conditions Test" at the beginning of this section.

The Test All diagnostic does not use or test the following circuits:

- Digital Inputs and Outputs (refer to "Digital Input Failures" in this section)
  A22 HP-IB (refer to A2, A22 CPU/HP-IB troubleshooting procedures in Section VIII)
- Trigger mode circuits (refer to "Isolating Trigger Failures" in this section for trigger failures)
- Auto Range Circuits (refer to "Self Calibration" in this section)
- Burst and noise source circuits (refer to "Source Failures" in this section)

Follow the Test All procedures beginning with Procedure One, "Test All Start", to isolate the failure.

Test All Procedure ONE - Test All Start

1. Press the line switch ON.
2. Press the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... RESULT
TEST ..... TEST
LOG

3. If the FPP, FFT, and Global RAM passed the power-up test, then these assemblies are probably operating correctly. If any of these assemblies failed the power-up test, refer to table 7-7.
4. Press the HP 3563A keys as follows:

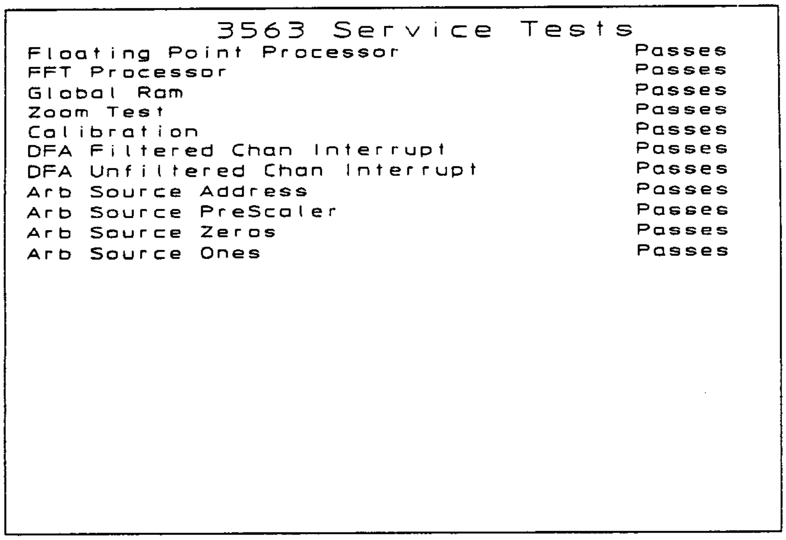
[Control]
PRESET ...... RESET

[Input Setup]
CAL ..... AUTO
ON OFF

[Control]
SPCL
FCTN ..... SERVIC
TEST ...... TEST
ALL

This test takes about two minutes to complete, if there are no failures. If there is a failure, it may take four minutes to complete. The test log is displayed when the self-tests are completed.

5. Refer to table 7-6 to verify the normal Test All result.
6. Use figure 7-7 after running the Test All diagnostic.



```
                    3563 Service Tests
Floating Point Processor                              Passes
FFT Processor                                         Passes
Global Ram                                            Passes
Zoom Test                                             Passes
Calibration                                           Passes
DFA Filtered Chan Interrupt                           Passes
DFA Unfiltered Chan Interrupt                         Passes
Arb Source Address                                    Passes
Arb Source PreScaler                                  Passes
Arb Source Zeros                                      Passes
Arb Source Ones                                       Passes
```

Figure 7-6. Test All Passes

Table 7-7. Test All Results

Tests not listed may either pass or fail(don't care). To use table, start with first line.

Test All Result	Go To
1. Test All passes	"Test All Table" in this section
2. Test All does not complete self-tests (test log is not displayed)	Test All Procedure TWO "Test All Does Not Complete"
3. FPP Fails	Replace A7 board See table 4-1 for the HP part number
4. FFT Fails	A9 FFT troubleshooting procedures in Section VIII
5. Global RAM Fails	Replace A38 board
6. Keyboard Status Test Fails	A15 Keyboard troubleshooting procedures in Section VIII
7. DFA Interrupt Fails	"Isolating Front End Failures" procedures in this section
8. DFA Unfiltered Chan Interrupt Fails	"Isolating Front End Failures" procedures in this section
9. Arb Source Fails	Isolating Front End Failures Procedure TWO, "Lo and Digital Source Check"
10. Source Test Fails, Calibration Fails, Front End Passes	"Source Failures" procedures in this section
11. Calibration Fails, Front End Passes, Source Test Passes	A30 Analog Source troubleshooting procedures in Section VIII
12. Calibration Fails, Front End Fails only on one channel, Source Test Passes	Isolating Front End Failures Procedure THREE, "Digital Check"
13. Source Test Fails, Front End Fails, Calibration Fails	"Isolating Front End Failures" procedures

Test All Table

Use table 7-8 to help determine the failure after running the Test All diagnostic or any individual self-tests. The table lists the self-tests in the order the Test All diagnostic executes them. A pass message indicates the assemblies and subblocks tested are probably operating correctly. The pass/fail messages are listed on the vertical axis of the table. The assemblies and subblocks tested or used by the self-tests are listed on the horizontal axis of the table. (Refer to the introduction of the Test All section for the list of assemblies not tested by Test All.)

There are two symbols used in table 7-8: O and X. When the symbol "O" is used in the table, the assembly or subblock is used in the test but is not a likely cause of the failure. When the symbol "X" is used in the table, the assembly or subblock is probably the cause of the failure. No symbol means the assembly or subblock is not used in the test.

Table 7-8. Test All Messages

The filled box means the assembly or subblock is the most likely cause of the failure message.

The symbol O means the assembly or sublock is used in the circuit but is not the most likely cause of the failure message.

No symbol means the assembly or subblock is not used in the test.

Note: Press SELF TEST ...SERVIC TEST ...TEST ALL to run all of the tests. To run individual tests press the key listed under the "Press Key" column.

Assembly/Subblock

Pass/ Fail Messages	Description	8 MHz Clock A2	+5S A18	System CPU A2	System Bus —	Program ROM A38	Global Bus —	Global RAM A38	Mother Board A14	±15S A18	Display Interface A17	Keyboard A15	FFP A7	FFT A9	+8S1, +8S2 A18	10.24 MHz Clock A31
Power-up Test Codes	See Table 7-6	O	O	O	O	O	O	O	O							
FFT "messages"	FFT Self-Test	O	O	O	O	O	O	O	O	O	O	O		▨		
FPP "messages"	FPP Self-Test	O	O	O	O	O	O	O	O	O	O	O	▨			
DFA Interrupt "messages"	DFA Interrupt Test	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Counter "bit#"	DFA Local Bus Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Local Bus "bit#"	DFA Local Bus Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
Calibration"messages"	Self-Calibration	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 1 Zoom Signal	Zoom Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 2 Zoom Signal	Zoom Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 1 Zoom Noise	Zoom Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 2 Zoom Noise	Zoom Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Source Distortion	Source Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Source Signal Level	Source Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Calibration Distortion	Source Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Calibration Signal Level	Source Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 1 Operation	Front End Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 2 Operation	Front End Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 1 Distortion	Front End Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Channel 2 Distortion	Front End Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Digital Source F/E Interface "bit#"	Digital Source Self Test	O	O	O	O	O	O	O	O	O	O	O				O
Digital Source Main Test "bit#"	Digital Source Self Test	O	O	O	O	O	O	O	O	O	O	O				O
ADC Channel 1 "messages"	ADC Tests	O	O	O	O	O	O	O	O	O	O	O			O	O
ADC Channel 2 "message"	ADC Tests	O	O	O	O	O	O	O	O	O	O	O			O	O
LO "messages"	LO Functional	O	O	O	O	O	O	O	O		O	O				O
DFA Functional Channel 1	Zoom with Square Wave Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
DFA Functional Channel 2	Zoom with Square Wave Test	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
DFA Channel 1 Real Filter	DFA Data Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Channel 1 Imaginary Filter	DFA Data Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Channel 2 Real Filter	DFA Data Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Channel 2 Imaginary Filter	DFA Data Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DMA "messages"	DFA DMA Bus Echo	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Filter Bus 1 "bit#"	DFA Filter Bus Test	O	O	O	O	O	O	O	O	O	O	O			O	O
DFA Filter Bus 2 "bit#"	DFA Filter Bus Test	O	O	O	O	O	O	O	O	O	O	O			O	O
ARB Source Fails	Digital I/O Test	O	O	O	O	O	O	O	O	O	O	O			O	O

Test All Messages continued

Digital Filter Controller	SYNC 2	Digital Filter Local Bus	Digital Filter Channel 1	Digital Filter Channel 2	DMA Controller	±15A	±30V	+5V Front end	Input Channel 1	Input Channel 2	Channel 1 Interface Shift Registers	Channel 2 Interface Shift Registers	20.48 MHz Clock	ADC Channel 1	ADC Channel 2	Calibrator	Main Source Output	Digital Source	Noise Generator	Front End Interface	Phase Resolution(BFST)	Local Oscillator	Digital I/O
A6	**A5**	**A5/ A6**	**A5**	**A5**	**A5**	**A18**	**A18**	**A18**	**A33**	**A35**	**A33**	**A35**	**A31**	**A32**	**A34**	**A30**	**A30**	**A1**	**A1**	**A1**	**A1**	**A4**	**A10**
O	O	O	O	O	O																		
▨	O	▨	O	O		O																	
▨	O	▨	O	O		O																	
O	O	O	O	O	O	O	O	O	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	O
O	O	O	▨		O	O	O	O	▨		O	O	O	▨	O		O	O		O	O	O	
O	O	O		▨	O	O	O	O		▨		O	O		▨		O	O		O	O	O	
O	O	O	▨		O	O	O	O	▨		O		O	▨			O	O		O	O	O	
O	O	O		▨	O	O	O	O		▨		O	O		▨		O	O		O	O	O	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O		▨	O		O	O	O	O
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O		▨	O		O	O	O	O
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	▨	O	O		O	O	O	O
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	▨	O	O		O	O	O	O
O	O	O	O		O	O	O	O	▨		O	O	O	▨	O	O	O	O		O	O	O	O
O	O	O		O	O	O	O	O		▨		O	O		▨	O	O	O		O	O	O	O
O	O	O	O		O	O	O	O	▨		O	O	O	▨	O	O	O	O		O	O	O	O
O	O	O		O	O	O	O	O		▨		O	O		▨	O	O	O		O	O	O	O
																		▨		▨			
																		▨		▨	▨		
O		O	O		O	O	O	O			O		O	▨				O		O			O
O		O		O	O	O	O	O				O	O		▨			O		O			O
	O																					▨	
O	O	O	▨		O																	▨	
O	O	O	O	▨	O																	▨	
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O			▨		O																		
O				▨	O																		
O	O	O	O	O	O								O		O			O		O	O	O	▨

Test All Procedure TWO - Test All Does Not Complete

Use this procedure when the test log is not displayed within 5 minutes after pressing TEST ALL.

1. Press the line switch OFF.
2. Remove the following assemblies:

   A5 Digital Filter
   A7 FPP
   A9 FFT
   A10 Digital I/O

Note To remove the A10 board, the side cable must be disconnected.

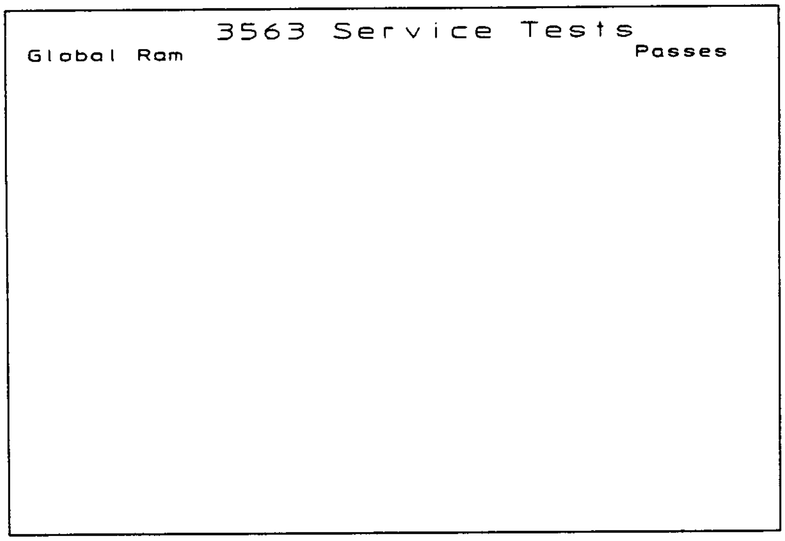
---

3. Press the line switch ON and the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC TEST ..... TEST MEMORY ..... GLOBAL RAM

If test fails or the display does not appear as in figure 7-7, replace the A38 assembly. See table 4-1 for the HP part number.

4. Press the line switch OFF.
5. Replace the A7 FPP assembly.



3563 Service Tests

Global Ram Passes

Figure 7-7. Global RAM Test Passes

6. Press the line switch ON and the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC TEST ...... TEST PROC
...... TEST FPP ...... FPP FUNCTN

If this test fails, replace the A7 board. See table 4-1 for the HP part number.

7. Press the line switch OFF.

8. Replace the A9 FFT assembly.

9. Press the line switch ON and the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC TEST ...... TEST PROC
...... TEST FFT ...... FFT FUNCTN

If this test fails, start with the A9 FFT troubleshooting procedures in Section VIII.

10. Press the line switch OFF.

11. Replace the A5 DGTL FLTR assembly.

12. Press the line switch ON.

13. Press the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... TEST
PROC
...... TEST
DFA ...... FILTER
TEST

If this test fails, replace the A5 board. See table 4-1 for the HP part number.

14. Press the line switch OFF.

15. Replace the A10 Dital I/O Board.

16. Press the line switch ON.

17. Press the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... TEST
SOURCE ..... ARBITARY

18. If the display is normal and the fault has not been found, go to the next section, "Isolating Front End Failures".

19. If the display is defective and the fault has not been found, go to the "Control Line Test" troubleshooting procedures appearing later in this section.

If this test fails go to Digital Input Failures.

Isolating Front End Failures

This procedure assumes the core assemblies are operating correctly and the Test All procedure was done. The self-diagnostic message "Front End Fails" can be caused by the following assemblies:

A1 Digital Source
A4 Local Oscillator
A5 Digital Filter
A6 Digital Filter Controller
A10 Digital I/O
A30 Analog Source
A32 Analog Digital Converter Channel 1
A33 Input Channel 1
A34 Analog Digital Converter Channel 2
A35 Input Channel 2
A31 Trigger

Note

For some failures it takes up to three minutes to complete a test. If a test takes more than five minutes to terminate (the test log is displayed), the test has failed.

Isolating Front End Failures Procedure ONE - Signal Check

1. Press the line switch OFF.
2. Remove the top cover.
3. Press the line switch ON.
4. After the power-up tests are completed, use a scope to verify the signals listed in table 7-9. If all the signals are operating correctly, go to step 5.

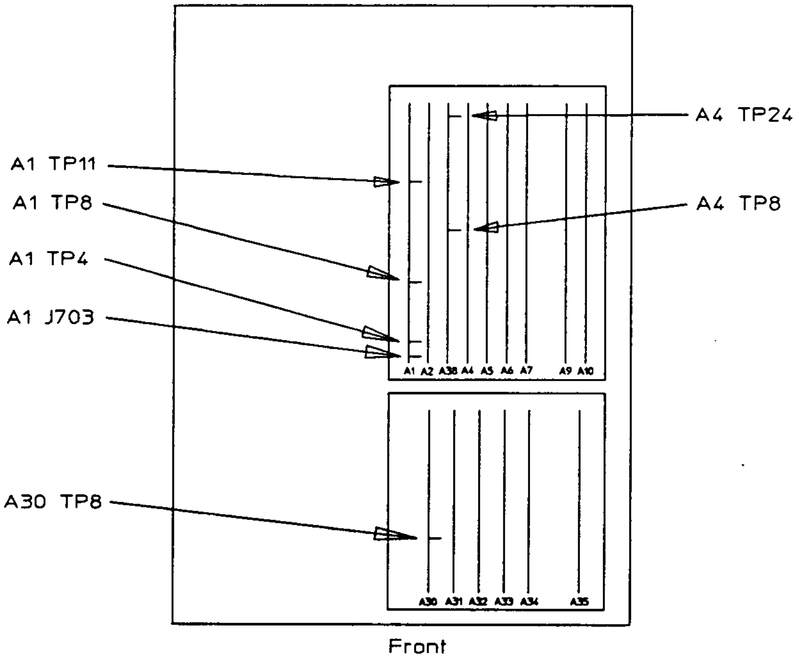


Figure 7-8. HP 3563A Top View, Cover Removed

Table 7-9. Front End Signal Check

Test Location	Signal Name	Waveform #	Probable Cause	Go To
A1 TP4	10.24 MHz	#2	A31 Trigger	A31 troubleshooting procedures in Section VIII
A1 TP8	SAMP	#5	A34 ADC 2	A32, A34 troubleshooting procedures in Section VIII
A1 J703-1	DREQL	#5	A5 Digital Filter A6 D FLTR CONT	See Below
A4 TP8	SYNC2	#6	A5 Digital Filter A6 D FLTR CONT A4 LO	SYNC2 Test, Procedure SIX
A4 TP24	COS	#6	A4 LO	See Below
Refer to step 5 for key presses to view CNTCLK.				
A1 TP11	CNTCLK	#4	A1 Digital Source	A1 troubleshooting procedures in Section VIII
Press A2 S1 to view the STIM@ waveform (STIM@ isdisabled when calibration is done).				
A30 TP8	STIM@	#8	A30 Analog Source	A30 troubleshooting procedures in Section VIII

A4, A5, A6, A7 and A17 board assemblies cannot be repaired to the component level. See table 4-1 for the HP part numbers.

5. Press the HP 3563A keys as follows:

⌈ Control ⌉
SPCL
FCTN ...... SERVIC
TEST ...... LOOP
ON OFF
...... TEST
SOURCE ...... FR END
INTFCE

6. After viewing the waveform, press A2 S1 (reset switch on A2 CPU).

Isolating Front End Failures Procedure TWO - LO and Digital Source Check

1. Press A2 S1 (reset switch on A2 CPU).

2. Press the HP 3563A keys as follows:

   [Control]
   SPCL
   FCTN ...... SERVIC
   TEST ...... TEST
   SOURCE ..... LO
   FUNCTION

3. If this test fails, Replace the A4 LO assembly.

4. If this test passes, the A4 Local Oscillator is probably working correctly.

5. Press the HP 3563A keys as follows:

   [Control]
   SPCL
   FCTN ...... SERVIC
   TEST ...... TEST
   SOURCE ..... SOURCE
   MAIN

6. When test is completed, note the test log message and then press:

   ...... FR END
   INTFCE

   If the Source main test or the Digital Source F/E interface test fails, start with the A1 Digital Source troubleshooting procedures in Section VIII.

   If these tests pass, the Digital Source interface circuits to the Inputs, ADC's, and Analog Source are probably operating correctly.

7. Continue fault isolation with Isolating Front End Failures Procedure THREE, "Digital Check".

Isolating Front End Failures Procedure THREE - Digital Check

1. Press the line switch OFF.
2. Pull the following assemblies up in their card nests:

   A32 ADC 1
   A33 INPUT 1
   A34 ADC 2
   A35 INPUT

3. Press the line switch ON.
4. Press the HP 3563A keys as follows:

   [Control]
   SPCL
   FCTN ...... SERVIC TEST ...... TEST PROC
   ...... TEST DFA ...... DFA FUNCTN

   If this test fails, replace the A5 and the A6 boards. See table 4-1 for the HP part numbers.

5. If this test passes, the A5 Digital Filter and A6 Digital Filter Controller assemblies are probably operating correctly. Replace all assemblies in their card nests.
6. Press the HP 3563A keys as follows:

   [Control]
   PRESET

   [Control]
   SPCL
   FCTN ..... SERVIC TEST ...... TEST SOURCE ..... ARBITRARY

7. When the tests are completed, note the test log messages and then press:

   ...... RETURN
   ...... TEST INPUT ...... DIGITAL
   ...... INTERN PATH

8. When the tests are completed, note the test log messages and then press:

...... RETURN

...... ADC ...... DIGITAL TEST

9. Refer to table 7-10 for a description of each test log message and instructions of what to do next.

Table 7-10. ADC or Digital I/O Test Log Messages

Message	What To Do Next
All Arb Source test Pass DIG Internal Path Passes ADC Gate Array Passes	The data path from the ADC through the Digital I/O to the Digital Filter is okay. The Digital I/O is probably okay. Go to Procedure FOUR, "Output Sine Check."
Any Arb Source test fails or Dig Internal Path fails ADC Gate Array Passes	The A10 Digital I/O is most likely failing. Replace the A10 Digital I/O.
All Arb Source tests pass Dig Internal Path Passes ADC Channel 2 Gate Array Passes ADC Channel 1 Fails	A34 ADC 1 is most likely failing. Go to A32, A34 troubleshooting procedures in Section VIII
Any Arb Source test fails or Dig Internal Path fails ADC Channel 2 Gate Array fails	Either the Digital I/O is failing or the A34 ADC 2. Go to Procedure FIVE, "Input, ADC and Digital I/O Failures."

Isolating Front End Failures Procedure FOUR - Output Sine Check

1. Connect a scope to the source output on the front panel. Set the scope as follows:

CH1 V/Div	2 V/Div
Coupling	dc
Time/Div	500 μs/Div
Trigger	CH1

2. Press the HP 3563A keys as follows:

[Measurement]		
SOURCE	**SOURCE LEVEL**	**5 V**
......	**FIXED SINE**	**1 kHz**

3. Refer to figure 7-9 to verify the correct result.

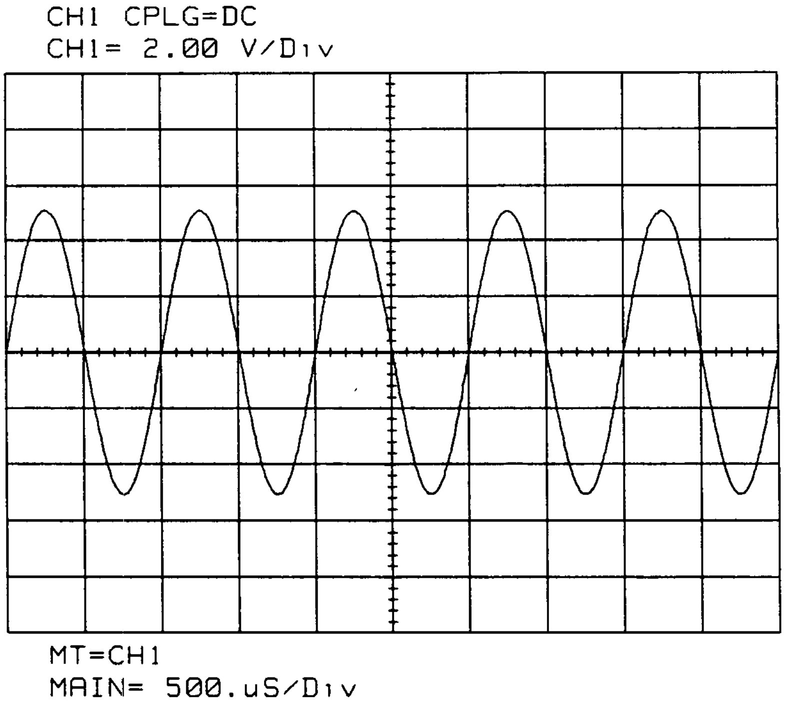


Figure 7-9. Sine Wave

4. If this test passes, the A4 Local Oscillator, the A1 Digital Source, and the A30 Analog Source are probably operating correctly, (except for chirp, noise, and trigger circuits).
5. Continue fault isolation with Procedure FIVE, “Input, ADC, and Digital I/O Failures.”

Isolation Front End Failures Procedure FIVE - Input, ADC, and Digital I/O Failures

This procedure isolates failures between the following assemblies:

A10 Digital I/O
A32 ADC 1
A33 INPUT 1
A34 ADC 2
A35 INPUT 2

The HP 3563A has two sets of identical assemblies: ADC 1 is identical to ADC 2 and Input 1 is identical to Input 2. This procedure interchanges these assemblies to aid in troubleshooting.

Note A failure on the ADC 2 board or the Digital I/O board may cause **both** channels to fail. Furthermore, the Input 1 board will not operate if the Input 2 board is removed.

---

1. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN      ......    SERVIC
                      TEST       ......    TEST
                                           INPUT
            ......    ADC        ......    DIGITAL
                                           TEST
```

2. When test is completed, note test log messages and then press:

```
            ......    FR END
                      FUNCT
```

3. When test is completed, note test log messages.
4. Press the line switch OFF.
5. Exchange the ADC 1 and the Input 1 pair with the ADC 2 and Input 2 pair.
6. Press the line switch ON and repeat step 1.
7. If the same channel fails as failed before the exchange, the most likely cause of the failure is the A10 Digital I/O assembly. Replace the assembly. Refer to table 4-1 for the HP part number.
8. Press the line switch OFF.
9. Exchange the ADC 1 board with the ADC 2 board.

10. Press the line switch ON and repeat step 1.

11. If the same channel fails as failed before the exchange, start troubleshooting with the input assembly for that channel (go to the A33, A35 Input troubleshooting procedures in Section VIII).

12. If the other channel now fails, start troubleshooting with the ADC assembly for that channel. Go to the A32, A34 ADC troubleshooting procedures in Section VIII.

13. The A30 Analog Source is the most likely cause of the failure **IF** the following are true:
    - The Signal Check passed (Procedure ONE).
    - The LO and Digital Source Check passed (Procedure TWO).
    - The Digital Check Passed (Procedure THREE).
    - Both channels failed, "FR END FUNCT" **before** the exchange.
    - Both channels failed, "FR END FUNCT" **after** the exchange.

14. Continue fault isolation with Procedure SIX, "SYNC2 Test."

Isolating Front End Failures Procedure SIX - SYNC2 Test

The A4 Local Oscillator will function without the A5 Digital Filter if the SYNC2 signal is activated. Perform this procedure to determine if the A5 Digital Filter is the cause of the failure.

1. Press the line switch OFF.
2. Remove the A5 Digital Filter.
3. Put the extender board in the A5 Digital Filter's card nest.
4. Connect a square wave to pin 16 on the extender board as follows:

Function	Square Wave
Frequency	250 kHz
Amplitude	5 Vpp
dc Offset	2.5 V

5. Press the line switch ON and press the HP 3563A keys as follows:

[Measurement]

SOURCE	......	SOURCE LEVEL	......	5 V		
SOURCE		TYPE	......	FIXED SINE	.....	1 kHz

6. Use a scope to verify COS at A4 TP24; table 7-31, Waveform #7.

   If this signal is not correct, replace the A4 assembly. See table 4-1 for the HP part number.

7. Connect the scope to the source output on the front panel. Set the scope as follows:

CH1 V/Div	2 V/Div
Coupling	dc
Time/Div	500 µs/Div
Trigger	CH1

8. Refer to figure 7-10 to verify the correct result.

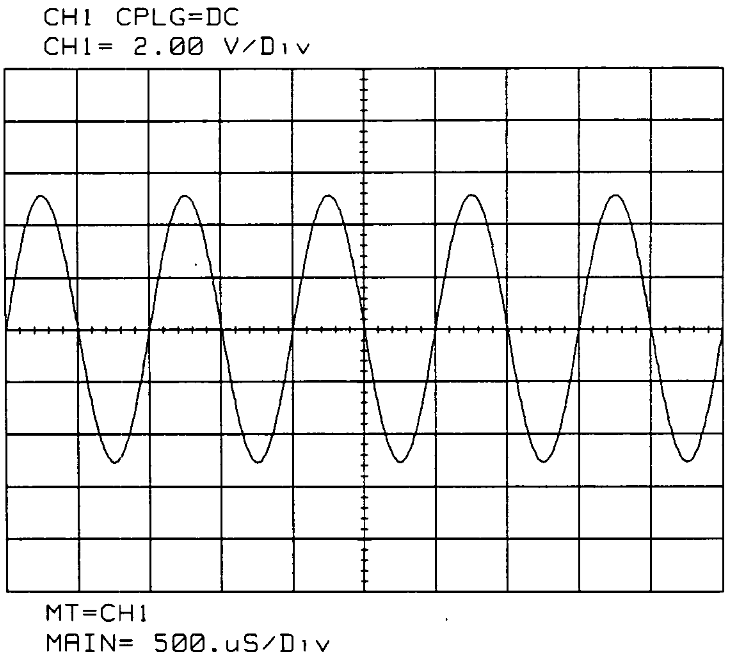


Figure 7-10. SYNC 2 Test Sine Wave

If this test fails, start with the A4 Local Oscillator troubleshooting procedures in Section VIII.

9. If this test passes, the A4 Local Oscillator, the A1 Digital Source, and the A30 Analog Source are probably operating correctly, (except for chirp, noise, and trigger circuits). If this test passes, the most likely cause of failure is the A5 Digital Filter assembly. Another possible cause of failure, although unlikely, is the A6 Digital Filter Controller assembly.

Note

If the cause of the failure has not been found, go to the "Control Line Tests" which appears later in this section.

Source Failures

Source output failures can be caused by the A1 Digital Source, the A4 Local Oscillator, the A10 Digital I/O or the A30 Analog Source. To isolate the defective assembly, follow the procedures beginning with the "Source Failures Start" procedure.

Source Failures Procedure ONE - Source Failures Start

1. If all the source functions are operating except the random noise and burst random, start with the A1 Digital Source troubleshooting procedures in Section VIII.
2. If all the source functions are operating except burst random, periodic chirp, or burst chirp, go to Procedure THREE, "Burst Failures."
3. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN     ......  SERVIC
                   TEST      ......  TEST
                                     SOURCE  .....  LO
                                                    FUNCTN
```

If this test fails, replace the A4 assembly. See table 4-1 for the HP part number.

4. If this test passes, the A4 Local Oscillator is probably working correctly.
5. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN     ......  SERVIC
                   TEST      ......  TEST
                                     SOURCE  .....  SOURCE
                                                    MAIN
```

6. When this test is finished press the keys as follows:

```
           ......  FR END
                   INTFCE
```

7. If the Source Main test or the Digital Source F/E Interface test fails, start with the A1 Digital Source troubleshooting procedures in Section VIII.

If these tests pass, the A1 Digital Source is probably working correctly.

8. Press the HP 3563A keys as follows:

[Control]
PRESET

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... TEST
SOURCE ..... ARBITRARY

9. When the test are completed, note the test log messages and then press:

...... RETURN
...... TEST
INPUT ...... DIGITAL
..... INTERN
PATH

The A10 Digital I/O is the most likely cause of the failure IF the following are true:

- The “LO FUNCTN” test passed.
- The “SOURCE MAIN” and “FR END INTFCE”passed.
- The DFA self-tests passed when TEST ALL was run.
- Any of the Arb Source tests failed or the Digital Internal test failed.

Source Failures Procedure TWO - Source Data

1. Use a logic probe or scope to verify the signals in table 7-11 are toggling between TTL level high and TTL level low.

Table 7-11. Source Data

Test Location	Signal Name	In/Out	Waveform #	Probable Causes
A4 TP24	COS	A4 Out	#6	A4 Local Oscillator
A4 TP16	NDAT	A4 Out	#9	A4 Local Oscillator
A4 TP17	NLD	A4 Out	#11	A4 Local Oscillator
A4 TP14	NDCK	A4 Out	#11	A4 Local Oscillator

2. If the "Source Failures Start" and the "Source Data", (Procedures ONE and TWO) passed; start with the A30 Analog Source troubleshooting procedures in Section VIII.

Source Failures Procedure THREE - Burst Failures

1. Press the line switch OFF.
2. Place the A1 Digital Source on the extender board. Connect the source output to the Channel 1 input.
3. Press the line switch ON.
4. Press the HP 3563A keys as follows:

[Measurement]		
SOURCE	SOURCE LEVEL	**5 V**
......	SOURCE TYPE	BURST CHIRP
[Display]		
MEAS DISP	FILTRD INPUT	TIME REC 1

5. Refer to figure 7-11 to verify a normal burst chirp.

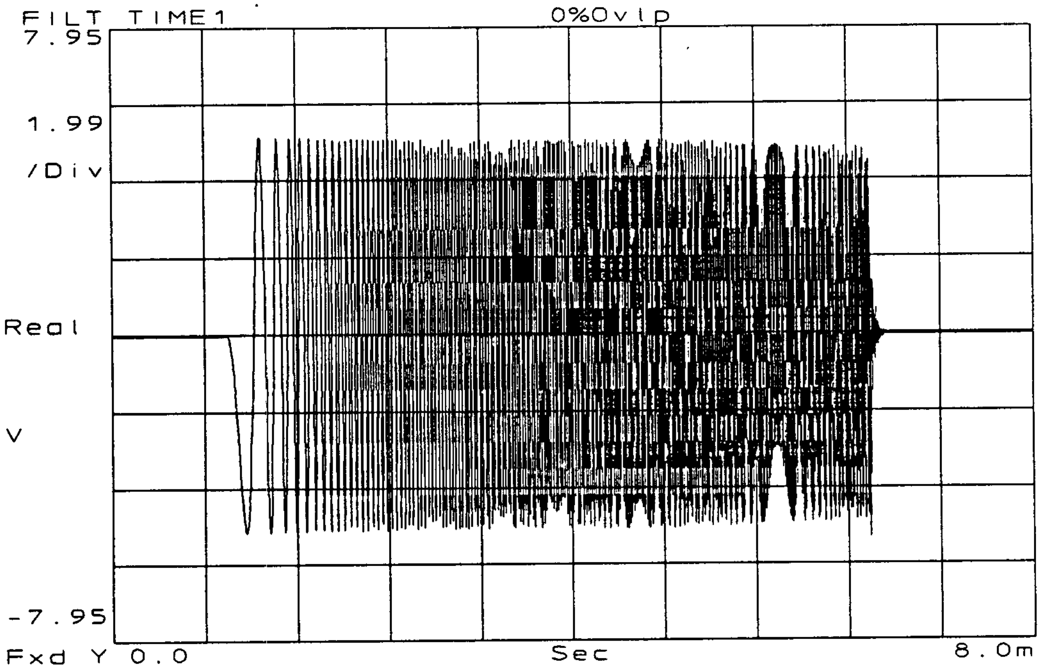


Figure 7-11. Burst Chirp

6. Use a scope and logic probe to verify the signals in table 7-12 are toggling between TTL level high and TTL level low. If any of the values are incorrect, go to Section VIII.

Table 7-12. Burst Mode Signals

Test Location	Signal	In/Out	Waveform Number	Probable Causes of Failure
A1 J701-3	NCLK	A1 Out	#12	A4 Digital Source
A1 J701-1	NSYNC	A4 Out	#12	A4 Local Oscillator
A1 J1-1	DACDAT	A1 Out	—	A4 Digital Source
A1 J1-5	BURSTEN	A1 Out	—	A4 Digital Source

Note

If NCLK fails, NSYNC also fails. Start with the A1 Digital Source troubleshooting procedures in Section VIII.

---

7. If the signals in table 7-12 are correct, start with the A30 Analog Source troubleshooting procedures in Section VIII.

Digital Input Failures

All the procedures in this section assume the failure has been isolated to the Digital Input section of the instrument. Digital input failures can be caused by one of the following:

A10 Digital I/O Board
A20 Connector Board
A21 Connector Board
External cables

The Arbitrary Self-Test and the Intern Path Self-test, test the A10 Digital I/O Board (including the digital source) without using the connector boards. If this test passes, the internal circuitry of the A10 assembly is most likely working. However, it does NOT test the A10's output circuitry to the connector boards, so the A10 board still could be the cause of the problem.

The Input Pod 1, the Input Pod 2, and the Qualfr Pod self-tests require external hookup to the A40 Test Board to run correctly. These self-tests, test most of the lines through the A10 input/output circuitry, connector boards, and cables. Refer to table 7-18 through table 7- 23 for a complete listing of the line connections between the A10 Board and the pod cables.

Digital I/O Test Setup Procedure

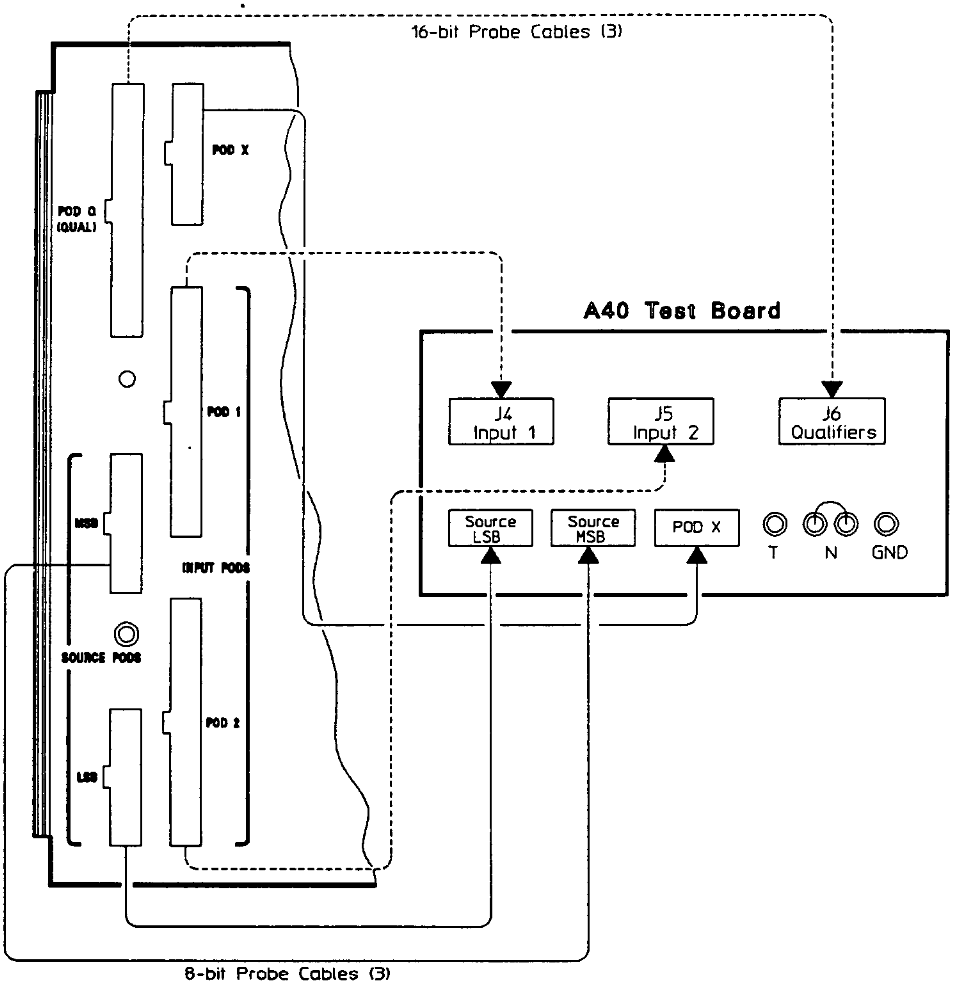


Figure 7-12. Digital Input/Output Test Setup

1. Press the line switch OFF.
2. Using the cables, connect the test board to the rear panel of the HP 3563A as shown in figure 7-12.
3. Verify the jumper is in the normal (N) position.
4. Press the line switch ON.

Arbitrary Self-Test

1. Press the HP 3563A keys as follows:

⌈ Control ⌉
PRESET

⌈ Control ⌉
SPCL
FCTN ...... SERVIC
TEST ...... TEST
SOURCE
..... ARBITRARY

If any failure messages are listed, the most likely cause of the failure is the A10 Digital I/O board.

Input and Qualifier Self-Test

1. Press the HP 3563A keys as follows:

⌈ Control ⌉
PRESET

⌈ Control ⌉
SPCL
FCTN ...... SERVIC
TEST ...... TEST
INPUT ..... DIGTAL

...... INTERN
PATH ..... INPUT
POD 1

..... INPUT
POD 2

..... QUALFR
POD

2. Use table 7-13 to help isolate the cause of the failure.

Table 7-13. Digital Input/Output Self-Tests

Message	Description and What to do Next
Dig Internal Path Fails	The most likely cause of the failure is the A10 Digital I/O Board
Src Clk Connection Fails	All the rest of the external tests will also fail. Verify the cables are connected to the test board properly and A40 J8 is in Normal (N) position. Rerun the test. If it still fails go to Digital I/O Manual Isolation Tests to further isolate the failure.
Dig Pod 1 Zeros Fails Bits: nn, mm, ...	There is an open in Dnn Go to Digital I/O Manual Isolation Tests.
Dig Pod 1 Ones Fails Bits: nn, mm, ...	There is a short in Dnn Go to Digital I/O Manual Isolation Tests.
Dig Pod 2 Zeros Fails Bits: nn, mm, ...	There is an open in Dnn Go to Digital I/O Manual Isolation Tests.
Dig Pod 2 Ones Fails Bits: nn, mm, ...	There is a short in Dnn Go to Digital I/O Manual Isolation Tests.
Dig Qualifier Zeros Fails Bits: nn, mm, ...	There is an open in Qnn, Qmm, Q... lines for the Qualifier. Go to Digital I/O Manual Isolation Tests.
Dig Qualifier Ones Fails Bits: nn, mm, ...	There is an short in Qnn, Qmm, Q... lines for the Qualifier.

Digital I/O Manual Isolation Tests

Digital I/O Cable Test

The 40 pin pod cables are interchangeable and the 20 pin pod cables are interchangeable.

1. Interchange the cable containing the failing line with one not failing.
2. Rerun the self-tests. Refer to table 7-18 through table 7-23 for the line connections.
3. If the failure moves, replace the cable.

Note The SRC CLK comes from POD X.

A10 Output Signal Check

1. Remove the instrument's right side cover (non-display side).
2. Remove the three long cables connected to A10 P101, P102, and P103.
3. Press the HP 3563A keys as follows:

[Control]
PRESET

[Control]
SPCL FCTN ...... **SERVIC TEST** ...... **TEST INPUT**
...... **DIGTAL**
...... **INPUT POD 1**

4. Verify the signals listed in table 7-14 while the self-test is running.

Note

The lines only toggle when the test is active. If the test completes before you finish, press the INPUT POD 1 softkey again .

Table 7-14. A10 Output Signal Check

A10 P103 Pin	TTL Level
(1)	Toggling
(3)	Low
(5)	Low
(7)	Toggling
A10 P101 Pin	**TTL Level**
(1)	Toggling
(3)	Toggling
(5)	Toggling
(7)	Toggling
(9)	Toggling
(11)	Toggling
(13)	Toggling
(15)	Toggling
A10 P102 Pin	**TTL Level**
(1)	Toggling
(3)	Toggling
(5)	Toggling
(7)	Toggling
(9)	Toggling
(11)	Toggling
(13)	Toggling
(15)	Toggling

If any of the signals are not correct, the most likely cause of the failure is the A10 Digital I/O Board.

A10 Input Signal Check

Note Only check the lines for the pod that is failing.

---

1. Remove the three short cables connected to A10 P1, P2, and P3.
2. Replace the three long cables connected to A10 P101, P102, and P103.
3. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN      ......   SERVIC
                     TEST      ......   TEST
                                        INPUT

                               ......   DIGTAL

                               ......   QUALFR
                                        POD
```

4. While the self-test is running, verify the signals from the Qualifier cable listed in table 7-15. The Qualifier cable is the short 24 pin cable that was connected to A10 P3.

Note The lines only toggle when the test is active. If the test completes before you finish, press the QUALFR POD again.

Table 7-15. A10 Input Signal Check – Qualifier Pod

Qualifier Cable Pin	TTL Level
(5)	Toggling
(7)	Toggling
(9)	Toggling
(11)	Toggling
(13)	Toggling
(15)	Toggling
(17)	Toggling
(19)	Toggling
(21)	Toggling
(23)	High

If any of the signals are not correct, the most likely cause of the failure is the A21 Connector Board.

5. Press the HP 3563A keys as follows:

[Control]
SPCL FCTN ...... SERVIC TEST ...... TEST INPUT
...... DIGTAL
...... INPUT POD 1

While the self-test is running, verify the signals from the Input 1 cable listed in table 7-16. The Input 1 cable is the short center 40 pin cable that was connected to A10 P1.

Note

The lines only toggle when the test is active. If the test completes before you finish, press the INPUT POD 1 softkey again.

Table 7-16. A10 Input Signal Check – Pod 1

Input Pod 1 Cable Pin	TTL Level
(7)	Toggling
(9)	Toggling
(11)	Toggling
(13)	Toggling
(15)	Toggling
(17)	Toggling
(19)	Toggling
(21)	Toggling
(23)	Toggling
(25)	Toggling
(27)	Toggling
(29)	Toggling
(31)	Toggling
(33)	Toggling
(35)	Toggling
(37)	Toggling

If any of the signals are not correct, the most likely cause of the failure is the A20 Connector Board.

6. Press the HP 3563A keys as follows:

[Control]
SPCL FCTN ...... SERVIC TEST ...... TEST INPUT
...... DIGTAL
...... INPUT POD 2

While the self-test is running, verify the signals from the Input 2 cable listed in table 7-17. The Input 2 cable is the short lower 40 pin cable that was connected to A10 P2.

Note

The lines only toggle when the test is active. If the test completes before you finish, press the INPUT POD 2 softkey again.

Table 7-17. A10 Input Signal Check – Pod 2

Cable Pin Input Pod 2	TTL Level
(7)	Toggling
(9)	Toggling
(11)	Toggling
(13)	Toggling
(15)	Toggling
(17)	Toggling
(19)	Toggling
(21)	Toggling
(23)	Toggling
(25)	Toggling
(27)	Toggling
(29)	Toggling
(31)	Toggling
(33)	Toggling
(35)	Toggling
(37)	Toggling

If any of the signals are not correct, the most likely cause of the failure is the A20 Connector Board.

If the inputs to the A10 Digital I/O Board are operating correctly, the most likely cause of the failure is the A10 Board.

Input/Output Cable Connections

Table 7-18. Signals from Input Pod 1 to A10

Signal Name	Connector A20 J1	Board A20 P1	Digital I/O A10 P1	A40 Test Board Signal Locations
Clock	(3)	(3)	(3)	R17
D15	(7)	(7)	(7)	R16
D14	(9)	(9)	(9)	R15
D13	(11)	(11)	(11)	R14
D12	(13)	(13)	(13)	R13
D11	(15)	(15)	(15)	R12
D10	(17)	(17)	(17)	R11
D9	(19)	(19)	(19)	R10
D8	(21)	(21)	(21)	R9
D7	(23)	(23)	(23)	R8
D6	(25)	(25)	(25)	R7
D5	(27)	(27)	(27)	R6
D4	(29)	(29)	(29)	R5
D3	(31)	(31)	(31)	R4
D2	(33)	(33)	(33)	R3
D1	(35)	(35)	(35)	R2
D0	(37)	(37)	(37)	R1

Table 7-19. Signals from Input Pod 2 to A10

Signal Name	Connector A20 J2	Board A20 P2	Digital I/O A10 P2	A40 Test Board
Clock	(3)	(3)	(3)	R34
D15	(7)	(7)	(7)	R33
D14	(9)	(9)	(9)	R32
D13	(11)	(11)	(11)	R31
D12	(13)	(13)	(13)	R30
D11	(15)	(15)	(15)	R29
D10	(17)	(17)	(17)	R28
D9	(19)	(19)	(19)	R27
D8	(21)	(21)	(21)	R26
D7	(23)	(23)	(23)	R25
D6	(25)	(25)	(25)	R24
D5	(27)	(27)	(27)	R23
D4	(29)	(29)	(29)	R22
D3	(31)	(31)	(31)	R21
D2	(33)	(33)	(33)	R20
D1	(35)	(35)	(35)	R19
D0	(37)	(37)	(37)	R18

Table 7-20. Signals from Qualifier Pod Cable to A10

Signal Name	Connector A21 J1	Board A21 P6	Digital I/O A10 P3	A40 Test Board Signal Locations
CLK	(3)	(3)	(3)	R44
TRG	(7)	(21)	(21)	R43
OVF	(9)	(23)	(23)	nc[1]
Q7	(23)	(5)	(5)	R42
Q6	(25)	(7)	(7)	R41
Q5	(27)	(9)	(9)	R40
Q4	(29)	(11)	(11)	R39
Q3	(31)	(13)	(13)	R38
Q2	(33)	(15)	(15)	R37
Q1	(35)	(17)	(17)	R36
Q0	(37)	(19)	(19)	R35

[1] No Connection

Table 7-21. Signals from A10 to Source MSB Pod Cable

Signal Name	A21 Connector Board						A10 Digital I/O	A40 Test Board
	J2		RN1		U1[2]	P3	P101	Signal Locations
		Out	In	Out	In			
S8	(1)	(16)	(1)	(18)	(2)	(1)	(1)	R9, R16, R43
S9	(3)	(15)	(2)	(17)	(3)	(3)	(3)	R10, R27
S10	(5)	(14)	(3)	(16)	(4)	(5)	(5)	R11, R28
S11	(7)	(13)	(4)	(15)	(5)	(7)	(7)	R12, R29
S12	(9)	(12)	(5)	(14)	(6)	(9)	(9)	R13, R30
S13	(11)	(11)	(6)	(13)	(7)	(11)	(11)	R14, R31
S14	(13)	(10)	(7)	(12)	(8)	(13)	(13)	R15, R32
S15	(15)	(9)	(8)	(11)	(9)	(15)	(15)	R16, R33

[2] A21 U1 is a buffer.

Table 7-22. Signals from A10 to Source LSB Pod Cable

Signal Name	A21 Connector Board						A10 Digital I/O	A40 Test Board
	P1		RN2		U2[3]	P4		
			In	Out	In			Signal Locations
S0	(1)	(16)	(1)	(18)	(2)	(1)	(1)	R1, R18, R35
S1	(3)	(15)	(2)	(17)	(3)	(3)	(3)	R2, R19, R36
S2	(5)	(14)	(3)	(16)	(4)	(5)	(5)	R3, R20, R37
S3	(7)	(13)	(4)	(15)	(5)	(7)	(7)	R4, R21, R38
S4	(9)	(12)	(5)	(14)	(6)	(9)	(9)	R5, R22, R39
S5	(11)	(11)	(6)	(13)	(7)	(11)	(11)	R6, R23, R40
S6	(13)	(10)	(7)	(12)	(8)	(13)	(13)	R7, R24, R41
S7	(15)	(9)	(8)	(11)	(9)	(15)	(15)	R8, R25, R42

[3] A21 U2 is a buffer.

Table 7-23. Signals from A10 to Pod X Cable

Signal Name	A20 Connector Board						A10 Digital I/O	A40 Test Board
	P3		RN1		U1[4]	P4	P103	
		Out	In	Out	In			Signal Locations
SRC CLK[5]	(1)	(15)	(2)	(18)	(2)	(1)	(1)	R17, R34, R44
SCE DAV	(3)	(14)	(3)	(17)	(3)	(3)	(3)	nc
SCE ENB	(5)	(13)	(4)	(16)	(4)	(5)	(5)	nc
SMP CLK	(7)	(12)	(5)	(15)	(5)	(7)	(7)	nc

[4] A20 U1 is a buffer.

[5] The SRC CLK is only connected when J8 is in Normal (N position.

Control Line Tests

Control line failures can cause false error codes and multiple failure messages. This procedure determines if a control line is defective.

Control Line Test ONE

1. Press the line switch OFF.
2. Place the A2 System CPU on the extender board.
3. Press the line switch ON.
4. Verify the RESETL line is a TTL level high at test point A2 U604-16.
5. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-24 are toggling between TTL level high and TTL level low.
6. If a line is TTL level stays low, go to "Control Line Test TWO".
7. Use table 7-24 to determine which assembly is defective.

Table 7-24. Control Lines Set #1

Test Location	Signal	In/Out	Probable Causes of Failure
A2 U500-1	IRQT4L	A9 Out	A2 CPU, A9 FFT
A2 U500-2	IRQT5L	A6 Out	A2 CPU, A6 D FLTR CONT
A2 U500-3	IRQT6L	A8 Out	A2 CPU, A38 MEM
A2 U500-13	IRQT3L	A7 Out	A2 CPU, A7 FPP
Press any key to toggle KYBRDL.			
A2 U604-3	KYBRDL	A2 Out	A2 CPU, A15 KFYBD
A2 U604-5	ASL	A2 Out	Any assembly on the system bus: A1 DGTL SCE, A2 CPU A4 LO, A6 D FLTR CONT A9 FFP, A10 DGTL I/O A15 KEYBD, A38 MEM
A2 U604-7	WRITEL	A2 Out	
A2 U604-9	UDSL	A2 Out	
A2 U604-12	LDSL	A2 Out	
A2 U604-14	VIOL	A2 Out	
A2 U508-4	DTACKL	A2 In	
A2 P1-11	ENBLL	A2 Out	A1 DGTL SCE, A2 CPU, A38 MEM, A4 LO
A2 U604-18	VMAL	A2 Out	
A2 U508-2	VPAL	A4 Out	A2 CPU, A4 LO
A2 U508-5	MR68L	A2 Out	A2 CPU, A38 MEM

Control Line Test TWO

1. Press the line switch OFF.
2. Remove one of the assemblies listed in table 7-25.
3. Press the line switch ON.
4. If the failing control line in table 7-24 is now toggling or TTL level high, the assembly removed is causing the failure.
5. Press the line switch OFF.
6. Replace the assembly.
7. Repeat steps 1 through 6 for the each of the remaining assemblies in table 7-25.

Table 7-25. Failing Control Line Assemblies

Reference Designation	Description
A1	Digital Source
A6	Digital Filter Controller[1]
A7	FPP
A9	FFT
A15	Keyboard[2]
A38	Memory[3]

[1] A5 Digital Filter must also be removed.
[2] Disconnect cable W10 from the A14 Mother board.
[3] MR68L should remain low with the Memory removed.

Control Line Test THREE

1. Press the line switch OFF.
2. Replace the A2 System CPU in its card nest. Place the A6 Digital Filter Controller on the extender board.
3. Press the line switch ON.
4. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-26 are toggling between TTL level high and TTL level low.

Table 7-26. Control Lines Set #3

Test Location	Signal	In/Out
A6 U304-6	BLDSL	A6 Out
A6 U304-7	BWRITEL	A6 Out
A6 U304-9	BUDSL	A6 Out

If any of the lines are not toggling, replace A6 assembly. Refer to table 4-1 for the HP part number.

5. Replace the A6 Digital Filter Controller in its card nest.

Isolating Trigger Failures

This procedure assumes the instrument operates correctly in the free run mode, but does not operate correctly in the trigger mode. Follow this procedure starting with the "Start" procedure to isolate the defective assembly.

Isolating Trigger Failures Procedure ONE – Start

1. If the trigger operates correctly except in external (EXT) trigger mode, start with the A31 Trigger troubleshooting procedures in Section VIII.
2. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN       ......    SERVIC
                       TEST        ......    TEST
                                             ALL
```

3. If any self-tests fail (except for calibration failures) go to the "Test All" procedures in this section.
4. Press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN       ......    SERVIC
                       TEST        ......    TEST
                                             SOURCE    .....    SOURCE
                                                                MAIN
```

5. When this test is finished press the keys as follows:

```
             ......    FREND
                       INTFCE
```

6. If the Source Main test or the Digital Source F/E Interface test fails, start with the A1 Digital Source troubleshooting procedures in Section VIII.
7. If the trigger operates correctly except in remote HP-IB trigger mode and the A1 Digital Source self-tests passed, with the A2,A22 System CPU HP-IB troubleshooting procedures in Section VIII.

Isolating Trigger Failures Procedure TWO

1. Use a BNC Tee to connect the front panel source output to Channel 1 and Channel 2.
2. Press the HP 3563A keys as follows:

⌈ Control ⌉						
PRESET						
⌈ Measurement ⌉						
SOURCE	......	SOURCE TYPE	......	SOURCE LEVEL	.....	**5V**
	......	FIXED SINE	......	**125**Hz		
⌈ Input Setup ⌉						
SELECT						
TRIG	......	CHAN 1 INPUT				
⌈ Display ⌉						
MEAS						
DISP	......	FILTRD INPUT	......	TIME REC1		
		SCALE	......	Y FIXD SCALE	.....	**−7, 7 V**

Refer to figure 7-13 to verify the correct result.

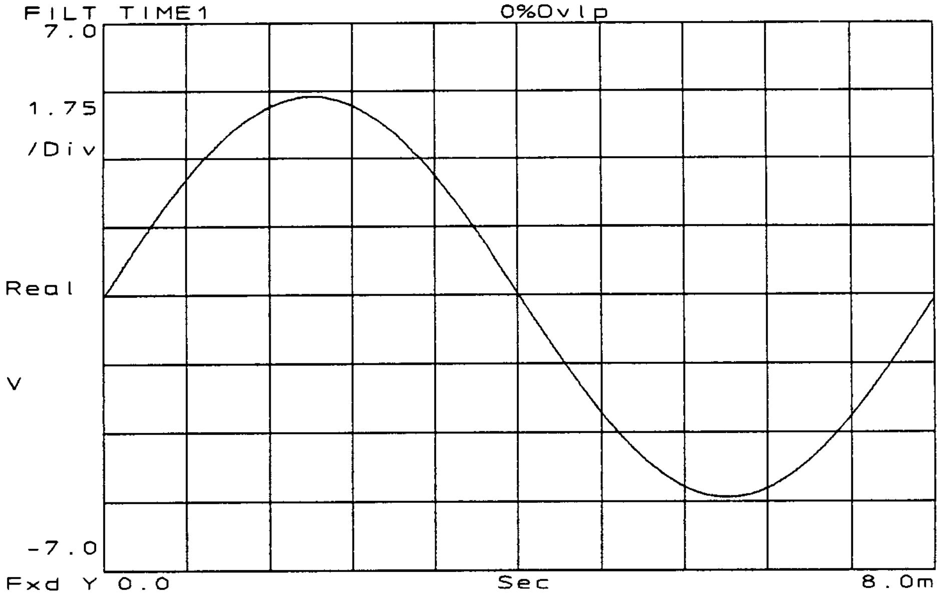


Figure 7-13. Triggered Sine Wave

Isolating Trigger Failures Procedure THREE

Press the HP 3563A keys as follows:

[Measurement]

SOURCE	......	SOURCE LEVEL	......	5V		
	......	SOURCE TYPE	......	FIXED SINE	.....	125Hz

[Input Setup]

SELECT TRIG	......	CHAN 2 INPUT

[Display]

MEAS DISP	......	FILTRD INPUT	......	TIME REC 2

[Display]

SCALE	......	Y FIXD SCALE	......	−7, 7 V

Refer to figure 7-13 to verify the correct result.

Isolating Trigger Failures Procedure FOUR

Use a scope to verify the signals TRIG IN and TRIGRO are operating correctly as shown in Waveform #14 (refer to table 7-31). If these signals are correct go to "Isolating Trigger Failures Procedure EIGHT".

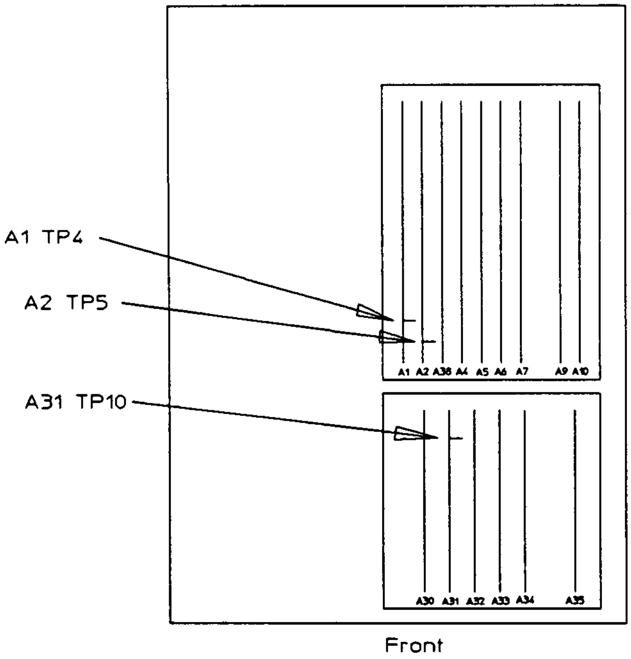


Figure 7-14. HP 3563A Top View, Cover Removed

Isolating Trigger Failures Procedure FIVE

1. Press the line switch OFF.
2. Put A32 ADC 1 on the extender board.
3. Press the line switch ON.
4. Repeat “Isolating Trigger Failures Procedure TWO.”
5. Use a scope to verify the signals in table 7-27 are operating correctly.

Table 7-27. Trigger Signal Check #5

Test Location*	Signal Name	In/Out	Waveform #	Probable Causes
A32 TP303	TRIG1@	A32 Out	#14	A32 ADC 1 (go to A32 troubleshooting procedures in Section VIII)
A31 TP3	TRIGIN	A31 Out	#14	A31 Trigger (go to A31 troubleshooting procedures in Section VIII)
A10 TP109	TRIGRO	A10 Out	#14	A10 Digital I/O

* Refer to figure 7-9.

Isolating Trigger Failures Procedure SIX

1. Press the line switch OFF.
2. Put the A32 ADC 2 on the extender board.
3. Press the line switch ON.
4. Repeat "Isolating Trigger Failures Procedure THREE."
5. Use a scope to verify the signals in table 7-28 are operating correctly.

Table 7-28. Trigger Signal Check #6

Test Location	Signal Name	In/Out	Waveform #	Probable Causes
A34 TP303	TRIG2@	A34 Out	#15	A34 ADC 2 (go to A32 troubleshooting procedures in Section VIII)
A31 TP3	TRIGIN	A31 Out	#15	A31 Trigger (go to A31 troubleshooting procedures in Section VIII)
A10 TP109	TRIGRO	A10 Out	#15	A10 Digital I/O

Isolating Trigger Failures Procedure SEVEN

Perform steps 1 through 4 as follows:

1. Press the line switch OFF.
2. Put A30 Analog Source on the extender board.
3. Press the line switch ON.
4. Use a scope to verify the signals in table 7-29 are operating correctly. Press A2 S1 (reset switch on A2 CPU) to view the STIM@ and CALTRIG waveforms (these signals are disabled when calibration is finished).

Table 7-29. Trigger Signal Check #7

Test Location	Signal Name	In/Out	Waveform #	Probable Causes
Press A2 S1 to view waveforms.				
A30 TP8	STIM@	A30 Out	#16	A30 ANLG SCE (go to A30 troubleshooting procedures in Section VIII)
A30 J30-19	CALTRIG	A30 Out	#16	A30 ANLG SCE go to A30 troubleshooting procedures in Section VIII)

Isolating Trigger Failures Procedure EIGHT

1. Press the line switch OFF.
2. Put the A1 Digital Source on the extender board.
3. Press the line switch ON.
4. Repeat "Isolating Trigger Failures Procedure TWO."
5. Use a logic probe or scope to verify the signals in table 7-30 are toggling between TTL level high and TTL level low.

Table 7-30. Trigger Signal Check #8

Test Location	Signal Name	In/Out
A1 TP9	BFST	A1 Out
A1 J1-83	ARML	A6 Out

6. Press the **PAUSE/CONT** key. ARML should now remain at TTL level high.
7. If ARML and BFST are operating correctly, replace thhe A6 assembly. See table 4-1 for the HP part number.
8. Press the line switch OFF.
9. Remove jumper A1 705. Connect a 6 Vpp, 1 kHz, 0 dc offset square wave to A1 J705-2.
10. Press the line switch ON.
11. Repeat "Isolating Trigger Failures Procedure TWO."

    If the instrument now triggers (the waveform may move around on the display), replace the A6 assembly. See table 4-1 for the HP part number.

    If the instrument still does not trigger, refer to the A1 Digital Source troubleshooting procedures in Section VIII.

Loop Mode and Intermittent Failures

Loop mode is used for some signature analysis tests and to find intermittent failures. Many intermittent failures can be isolated by running the self-tests in this mode. When the loop mode is activated, the instrument continually repeats a test until power is cycled, the loop mode is shut off, or a failure is found. Most of the self-tests can be run in loop mode. Run one of the following self-tests in loop mode to help isolate intermittent failures:

TEST ALL
HP-IB DIAG
FFT FUNCTN
FPP FUNCTN
GLOBAL RAM
ARBITRARY
INPUT POD 1
QUALFR POD
PROG ROM
SOURCE FUNCTN
LO FUNCTN
FR END FUNCTN
DIGTAL TEST
INTERN PATH
INPUT POD 2

Note Input Pod 1, Input Pod 2 and the Qualfr Pod self-tests require external hookups. Refer to "Digital Input Failures" in this section.

Use the "Spcl Fctn Key Map", figure 7-15, for the location of the service test keys.

Turning Loop Mode On/Off

1. To turn the loop mode on, press the following HP 3563A softkeys:

[Input Setup]
CAL ...... AUTO
ON OFF

[Input Setup]
RANGE ...... 0 dBV

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... LOOP
ON OFF

2. Press the keys to start a self-test. Failures of a test are entered in the test log, the self-test stops, and the test log is displayed.

3. To turn the loop mode off press A2 S1 (reset switch on A2 CPU) or press the keys as follows:

RETURN ...... LOOP
ON OFF

Note

Test All may fail the Channel 1 or Channel 2 zoom noise test after running for approximately 48 hours. The DFA Functional Test (**DFA Functn**) Filter Test (**Filter Test**) may fail the zoom noise test after running for approximately 2 hours. No other tests fails. This failure message results from a software anomaly and does not mean there is a hardware failure. Here is an example of the **Test All** failure message resulting from this problem.

Floating Point Processor		Passes
Global Ram		Passes
	Channel 1 Zoom, Signal	Passes
	Channel 2 Zoom, Signal	Passes
	Channel 1 Zoom, Noise	Passes
	Channel 2 Zoom, Noise	**FAILS**
Zoom Test		**FAILS**
Source Test		Passes
Front End		Passes
Calibration		Passes
DFA Filtered Channel Interrupt		Passes
DFA Unfiltered Channel Interrupt		Passes
DFA Functional Test		Passses

Troubleshooting Hints

1. Common causes of intermittent failures are:

   Cold solder joints
   Loose cables
   ICs loose in sockets
   Loose screws on power supply
   An assembly partially out of its card nest
   Overheating

2. An intermittent failure in the instrument can be caused by an assembly's bottom connector that attaches the assembly to the A14 Mother Board. Check for loose pins on the connector.

3. If the instrument intermittently powers down or fails to power up, the most likely cause is the power supply control circuits (go to A18 troubleshooting procedures in Section VIII).

4. Intermittent keyboard failures can be caused by the ribbon cable (W10) between the A15 Keyboard and A14 Mother Board.

5. Intermittent digital input and output failures can be caused by the external ribbon cables or pods.

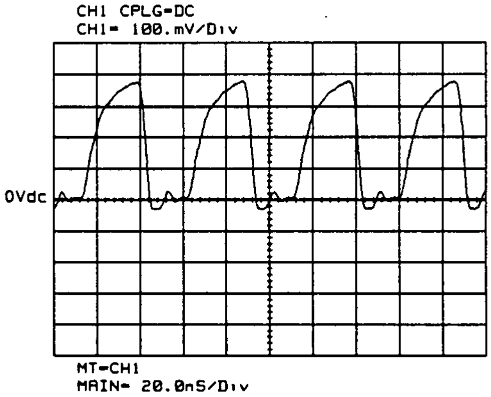
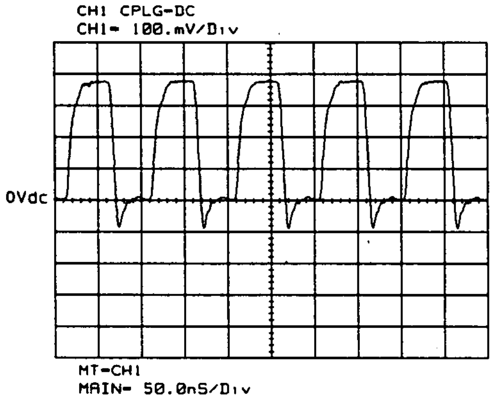
Waveforms

Waveforms

Use these waveforms to verify operation at various test points in the instrument. All oscilloscope measurements are taken using a 10:1 probe. Notes unique to a measurement are written next to the waveform.

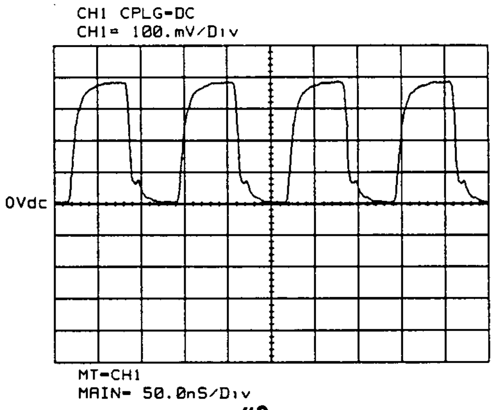
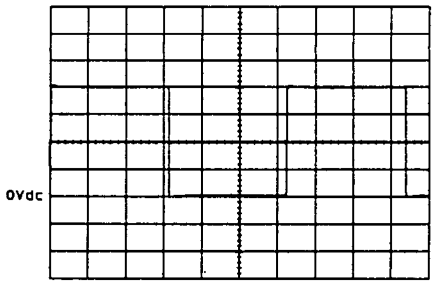
Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Table 7-31. Instrument Waveforms

All jumpers should be in normal position Probe 10:1		
Setup	**Parameters**	**Waveform**
20.48 MHz Connect CH1 to A31 TP10 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 20 ns/Div Trigger CH1	Time Pulse shape	 #1
10.24 MHz Connect CH1 to A1 TP4 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 50 ns/Div Trigger CH1	Time Pulse shape	 #2

Instrument Waveforms continued

All jumpers should be in normal position
Probe 10:1

Setup	Parameters	Waveform
8 MHz Connect CH1 to A2 TP5 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 50 ns/Div Trigger CH1	Time Pulse shape	 **#3**
Press the keys as follows to view CNTCLK: SPCL FCTN ...... SERVIC TEST ...... LOOP ON OFF TEST SOURCE ..... FR END INTFCE		
CNTCLK Connect CH1 to A1 TP11 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 10 μs/Div Trigger CH1	Time	 **#4**
Press A2 S1 (reset switch on A2 CPU) after viewing waveform.		

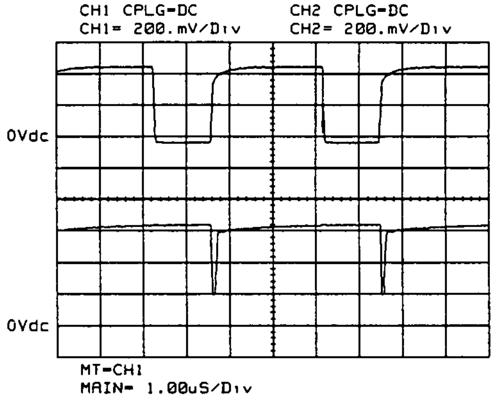
Instrument Waveforms continued

<table>
<tr><td colspan="3">All jumpers should be in normal position
Probe 10:1</td></tr>
<tr><th>Setup</th><th>Parameters</th><th>Waveform</th></tr>
<tr>
<td><b>SAMP and DREQL</b>

Connect CH1 to A1 TP8
Connect CH2 to A1 J703-1

Oscilloscope:

CH1 V/Div 200 mV/Div
CH2 V/Div 200 mV/Div
CH1 Coupling dc
CH2 Coupling dc

Time/Div 1 μs/Div
Trigger CH1</td>
<td>Time</td>
<td>

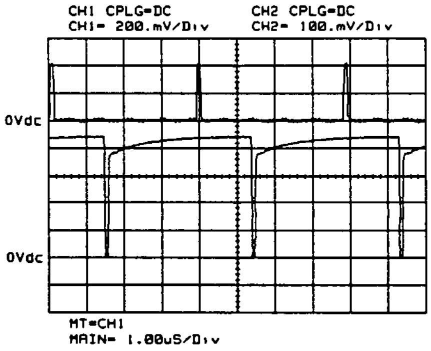
<b>#5</b></td>
</tr>
<tr>
<td><b>SYNC2 and COS</b>

Connect CH1 to A4 TP8
Connect CH2 to A4 TP24

Oscilloscope:

CH1 V/Div 200 mV/Div
CH2 V/Div 100 mV/Div
CH1 Coupling dc
CH2 Coupling dc

Time/Div 1 s/Div
Trigger CH1</td>
<td>Time

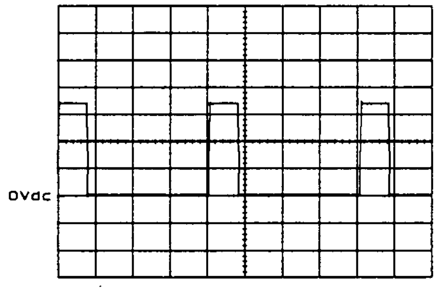
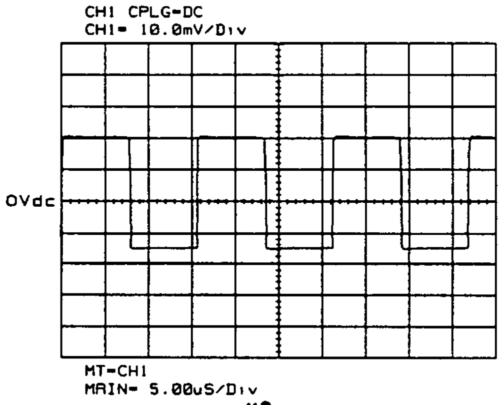
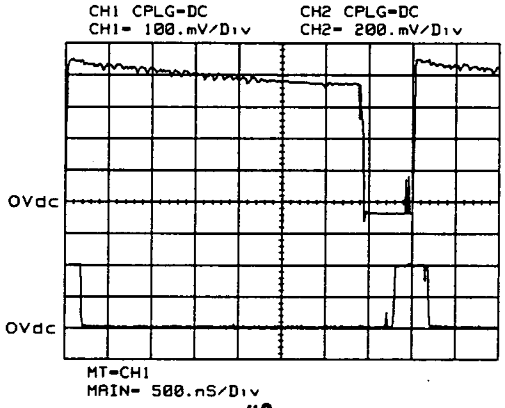
Pulse shapes</td>
<td>

<b>#6</b></td>
</tr>
</table>

(NOTE: Press A2S2 to view waveforms)

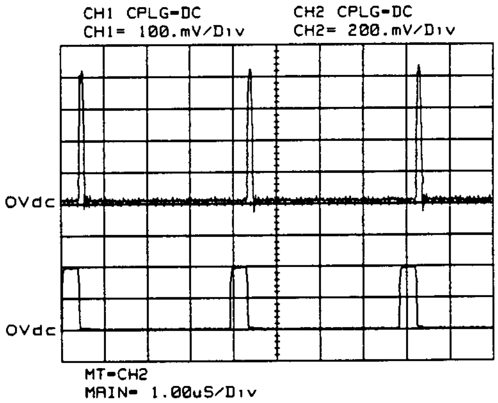
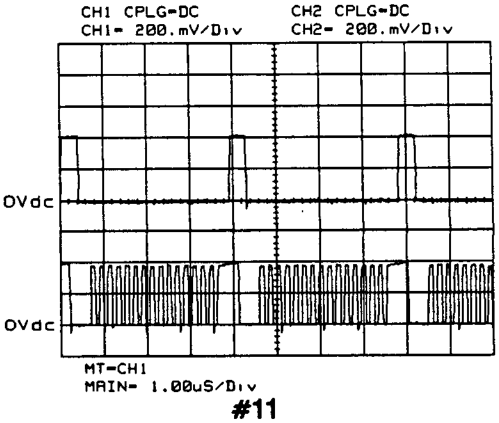
Instrument Waveforms continued

All jumpers should be in normal position
Probe 10:1

Setup	Parameters	Waveform
Refer to the SYNC2 Test for setup (Isolating Front End Failures Procedure Six).		
COS (no DFA) Connect CH1 to A4 TP24 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 μs/Div Trigger CH1	Time Pulse shape	 **#7**
Press A2 S1 to view STIM@.		
STIM@ Connect CH1 to A30 TP8 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 10 mV/Div CH1 Coupling dc Time/Div 5 μs/Div Trigger CH1	Time Pulse shape Amplitude	 **#8**
NDAT and NLD Connect CH1 to A4 TP16 Connect CH2 to A4 TP17 Oscilloscope: CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH1 Coupling dc Time/Div 500 ns/Div Trigger CH1	Time relationship	 **#9**

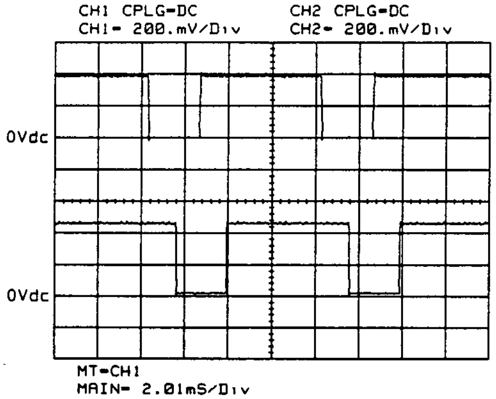
Instrument Waveforms continued

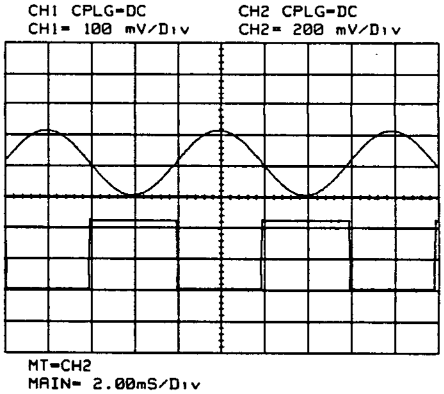
All jumpers should be in normal position
Probe 10:1

Setup	Parameters	Waveform
SYNC2 and NLD Connect CH1 to A4 TP8 Connect CH2 to A4 TP17 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH2	Time relationship	 **#10**
NLD and NDCK Connect CH1 to A4 TP17 Connect CH2 to A4 TP14 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH1	Time Relationship	 **#11**

Instrument Waveforms continued

All jumpers should be in normal position
Probe 10:1

<table>
<tr><th>Setup</th><th>Parameters</th><th>Waveform</th></tr>
<tr><td colspan="3">Press the keys as follows to view NSYNC and NCLK:
SOURCE ...... SOURCE LEVEL ...... 5 V
...... SOURCE TYPE ...... BURST CHIRP</td></tr>
<tr><td><b>NSYNC and NCLK</b>
Connect CH1 to A1 J701-1
Connect CH2 to A1 J701-3
Oscilloscope:
CH1 V/Div 200 mV/Div
CH2 V/Div 200 mV/Div
CH1 Coupling dc
CH2 Coupling dc
Time/Div 2 ms/Div
Trigger CH1</td><td>Time</td><td>

#12</td></tr>
<tr><td colspan="3">Refer to "Isolating Trigger Failures" for the HP 3563A input and key presses to view TRIGGER INPUT and TRIGIN.</td></tr>
<tr><td><b>TRIGGER INPUT and TRIGIN</b>
Connect CH1 to A31 TP1
Connect CH2 to A31 TP3
Oscilloscope:
Bandwidth Limit: ON
CH1 V/Div 100 mV/Div
CH2 V/Div 200 mV/Div
CH1 Coupling dc
CH2 Coupling dc
Time/Div 2 ms/Div
Trigger CH2</td><td>Time Relationship
Pulse shape</td><td>

#13</td></tr>
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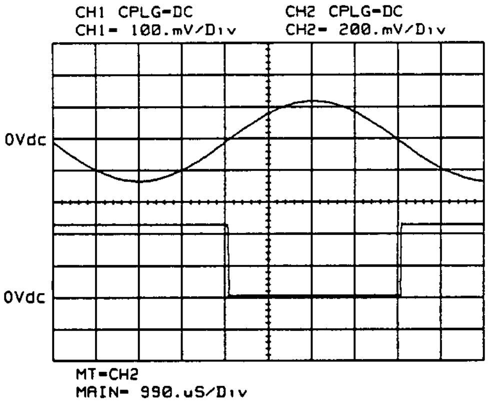
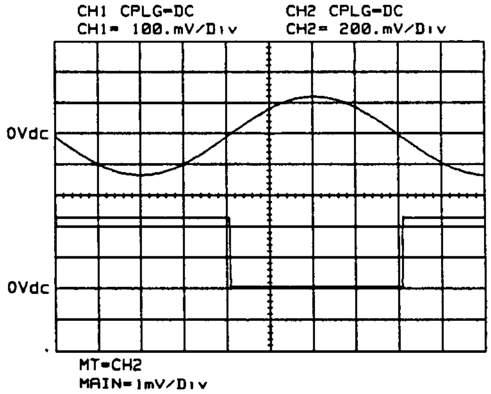
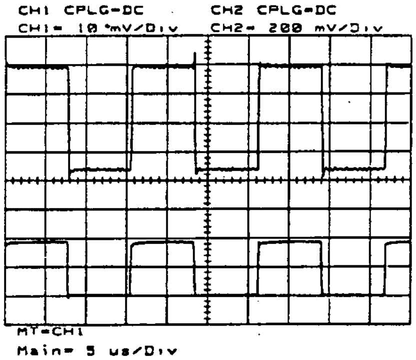
Instrument Waveforms continued

<table>
<tr><td colspan="3">All jumpers should be in normal position
Probe 10:1</td></tr>
<tr><th>Setup</th><th>Parameters</th><th>Waveform</th></tr>
<tr><td colspan="3">Refer to “Isolating Trigger Failures” for the HP 3563A input and key presses to view TRIG1@ and TRIGRO.</td></tr>
<tr><td><b>TRIG1@ and TRIGRO</b>
Connect CH1 to A32 TP303
Connect CH2 to A31 TP3 or A10 TP109
Oscilloscope:
Bandwidth Limit: ON
CH1 V/Div 100 mV/Div
CH2 V/Div 200 mV/Div
CH1 Coupling dc
CH2 Coupling dc
Time/Div 1 ms/Div
Trigger CH2</td><td>Time Relationship
Pulse shape</td><td>
#14</td></tr>
<tr><td colspan="3">Refer to “Isolating Trigger Failures” for the HP 3563A input and key presses to view TRIG2@ and TRIGRO.</td></tr>
<tr><td><b>TRIG2@ and TRIGRO</b>
Connect CH1 to A34 TP303
Connect CH2 to A31 TP3 or A10 TP109
Oscilloscope:
Bandwidth Limit: ON
CH1 V/Div 100 mV/Div
CH2 V/Div 200 mV/Div
CH1 Coupling dc
CH2 Coupling dc
Time/Div 1 ms/Div
Trigger CH2</td><td>Time Relationship
Pulse shape</td><td>
#15</td></tr>
</table>

Instrument Waveforms continued

All jumpers should be in normal position
Probe 10:1

Setup	Parameters	Waveform
Press A2 S1 to view STIM@ and CALTRIG.		
STIM@ and CALTRIG Connect CH1 to A30 TP8 Connect CH2 to A30 J30-19 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 10 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 5 s/Div Trigger CH1	Time Relationship Pulse shape	 **#16**

SPCL FCTN
Key Fctn

SPCL FCTN Key Map

Figure 7-15 illustrates the location of all the service test keys. Use the key map to find the key for a particular self-test. All keys marked in bold perform a self-test or a group of self-tests. Other soft keys are either used to reach the next level of soft keys or are used for other purposes such as adjustments and signature analysis.

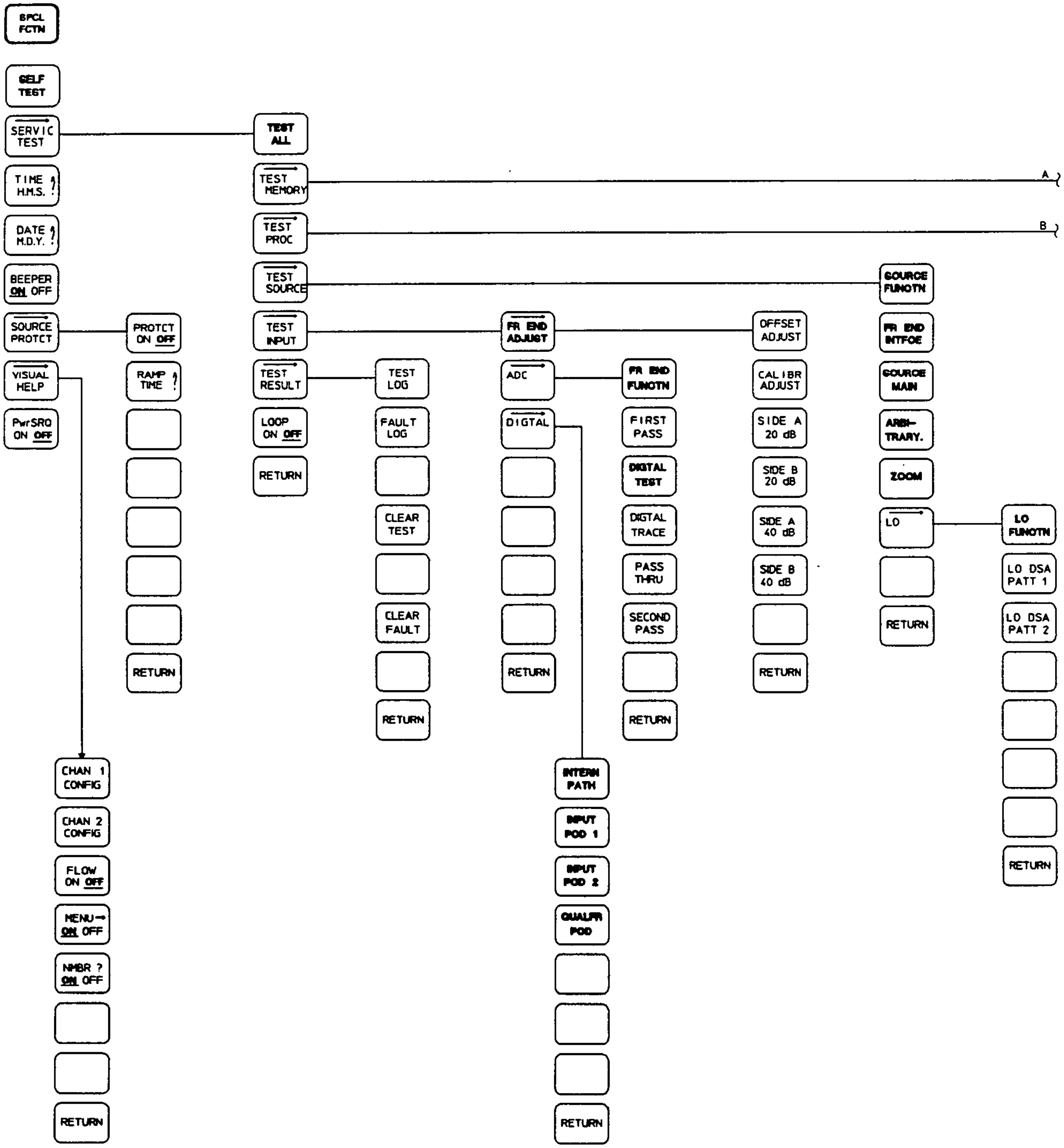
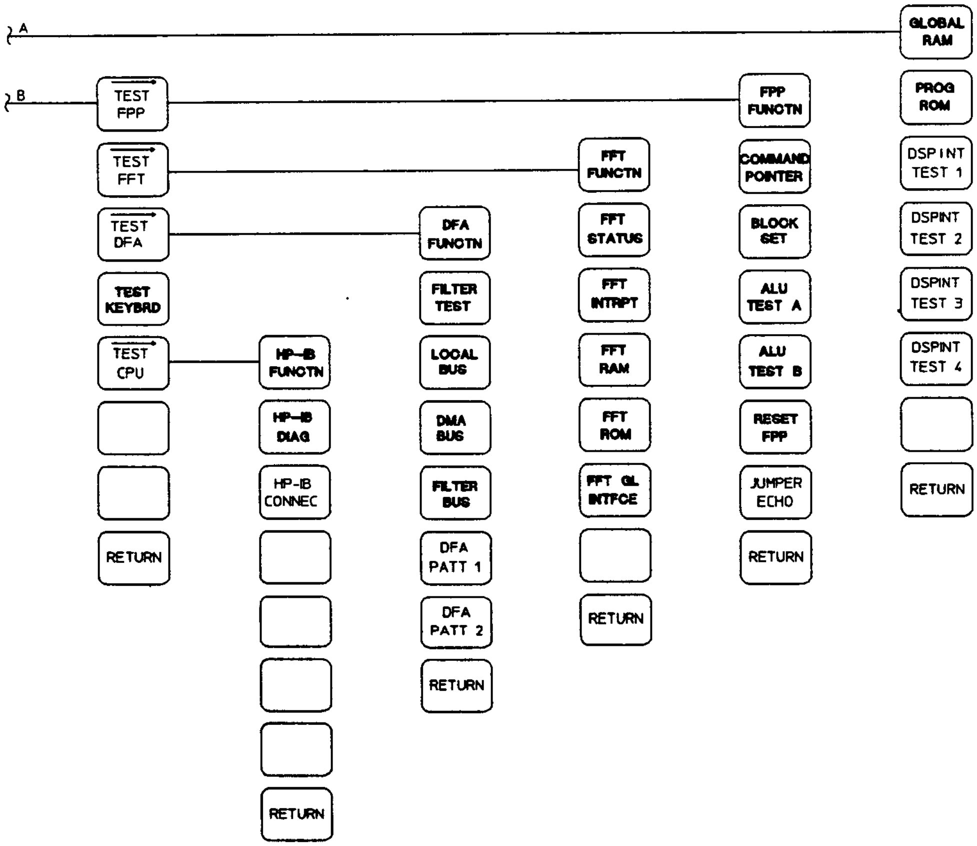


Figure 7-15. SPCL FCTN Key Map


A
B
TEST FPP
TEST FFT
TEST DFA
TEST KEYBRD
TEST CPU
RETURN
HP-IB FUNCTN
HP-IB DIAG
HP-IB CONNEC
RETURN
DFA FUNCTN
FILTER TEST
LOCAL BUS
DMA BUS
FILTER BUS
DFA PATT 1
DFA PATT 2
RETURN
FFT FUNCTN
FFT STATUS
FFT INTRPT
FFT RAM
FFT ROM
FFT GL INTFCE
RETURN
FPP FUNCTN
COMMAND POINTER
BLOCK SET
ALU TEST A
ALU TEST B
RESET FPP
JUMPER ECHO
RETURN
GLOBAL RAM
PROG ROM
DSP INT TEST 1
DSPINT TEST 2
DSPINT TEST 3
DSPINT TEST 4
RETURN

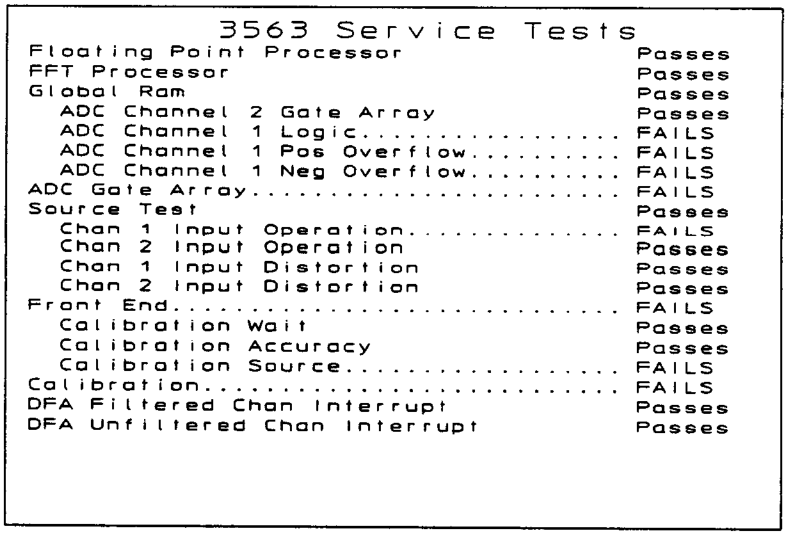
Test Log and Fault Log Descriptions

Test Log

The test log is a record of the results of the last self-test run. Pass and fail messages are entered in the test log while a self-test is running. The results of the power-up tests are also entered in the test log. If a self-test stops before finishing or to verify the result of the power-up tests, the test log can be read by pressing the keys as follows:

[Control]
SPCL
FCTN ..... SERVICE TEST ...... TEST RESULT ..... TEST LOG

If a self-test fails, error messages are listed for each test, then the test name is listed. For example (figure 7-16), the Gate Array Test only failed on Channel 1 when the test was performed in the TEST ALL sequence.



```
                   3563 Service Tests
Floating Point Processor                          Passes
FFT Processor                                     Passes
Global Ram                                        Passes
   ADC Channel 2 Gate Array                       Passes
   ADC Channel 1 Logic........................... FAILS
   ADC Channel 1 Pos Overflow.................... FAILS
   ADC Channel 1 Neg Overflow.................... FAILS
ADC Gate Array................................... FAILS
Source Test                                       Passes
   Chan 1 Input Operation........................ FAILS
   Chan 2 Input Operation                         Passes
   Chan 1 Input Distortion                        Passes
   Chan 2 Input Distortion                        Passes
Front End........................................ FAILS
   Calibration Wait                               Passes
   Calibration Accuracy                           Passes
   Calibration Source............................ FAILS
Calibration...................................... FAILS
DFA Filtered Chan Interrupt                       Passes
DFA Unfiltered Chan Interrupt                     Passes
```

Figure 7-16. Test Log Example

Fault Log

The fault log lists the A2 System CPU run-time errors or discrepancies. It also gives the revision code of the software that is in the instrument. Only assemblies that use the system bus generate fault log error messages, however, an HP-IB programming error or a failure on any assembly may cause a fault log entry. Use the fault log as a supplement to the fault isolation procedure. To read the test log press the keys as follows:

[Control]
SPCL
FCTN ...... SERVICE
TEST ...... TEST
RESULT ..... FAULT
LOG

Fault log messages accumulate in the fault log until the log is cleared. Use table 7-32 to interpret fault log messages.

Note

Using beeper commands other than those specified in this manual may result in a "software fault" entry in the fault log.

Table 7-32. System CPU Address Map

Data Address		Description		
From	To	Fault	Assembly Generating Message	Possible Assemblies Failing
000000000	000007FFF	Monitor ROM	A2	A2
00003D000	000040FFF	Program RAM	A2	A2
000060000	00007FFFF	Data RAM	A38	A2, A8
000D00000	000F3FFFF	Program ROM	A38	A2, A3
000FF81E0	000FF81FF	Digital I/O	A10	A2, A3, A10
0FFFF8001	0FFFF800F	HP-IB	A2	A2, A22
0FFFF8011	0FFFF801F	Programmable Timer	A2	A2
0FFFF8100	0FFFF8104	Display	A38	A2, A8, A17
0FFFF8121	0FFFF8127	Keyboard	A15	A2, A15
0FFFF8140	0FFFF8142	FPP	A7	A2, A7
0FFFF8160	0FFFF817E	IBC	A6	A2, A5, A6, A31
0FFFF8180	0FFFF818F	Front End CONA Timeout Trig Phase Error	A1	A1, A2, A3, A4, A5, A6
0FFFF81A1	0FFFF81AF	LO Lcl Oscil.	A4	A1, A2, A3, A4, A5, A6, A31, A32, A34
0FFFF81C0	0FFFF81CE	FFT	A9	A2, A9
—	—	Cal Failure	—	Any assembly

Diagnostic Descriptions

The self-tests consist of approximately 40 different tests that are run either in groups or individually to test a particular assembly, a function, or the entire instrument. The power-up tests are executed on turn-on, and the rest of the self-tests are invoked by pressing softkeys. This section describes the sequence of tests executed in groups and the SERVIC TEST softkey tests. Refer to table 7-4, "Power-up Test Codes", and table 7-6, "TEST ALL Messages", for a general description of the test result messages. For a detailed explanation of test result messages, refer to the troubleshooting paragraph for the failing assembly.

Power-Up Tests

The power-up tests consist of two sets of tests, low-level and high-level. The low-level tests exercise the A2 System CPU, the A38 Memory (Program ROM and Global RAM), the global bus, and the system bus. Fault and pass codes for these assemblies are displayed using the A2 System CPU test LEDs (A2 DS3, A2 DS4). The high-level tests exercise the A9 FFT, A7 FPP, A5 DGTL FLTR, and A6 D FLTR CONT assemblies. Faults on these assemblies are displayed in the test log. The instrument performs a calibration if the power-up tests pass. Refer to figure 7-17 for the Power-Up sequence.

Service Test Softkeys

This section describes the function of each of the service test softkeys. Refer to figure 7-15, "SPCL FCTN Key Map," for the location of each of the softkeys. Refer to Section VII and Section VIII for information on how to use the service test softkeys to isolate a failure.

SELF TEST

The SELF TEST key invokes a sequence of self-tests that thoroughly exercises the digital and analog hardware of the instrument. This test is designed to be used by the user to determine if the instrument is functioning correctly. If this self-test sequence fails, the failure is entered in the test log and "Self Test Fails" is displayed. Refer to figure 7-18 for the SELF TEST sequence.

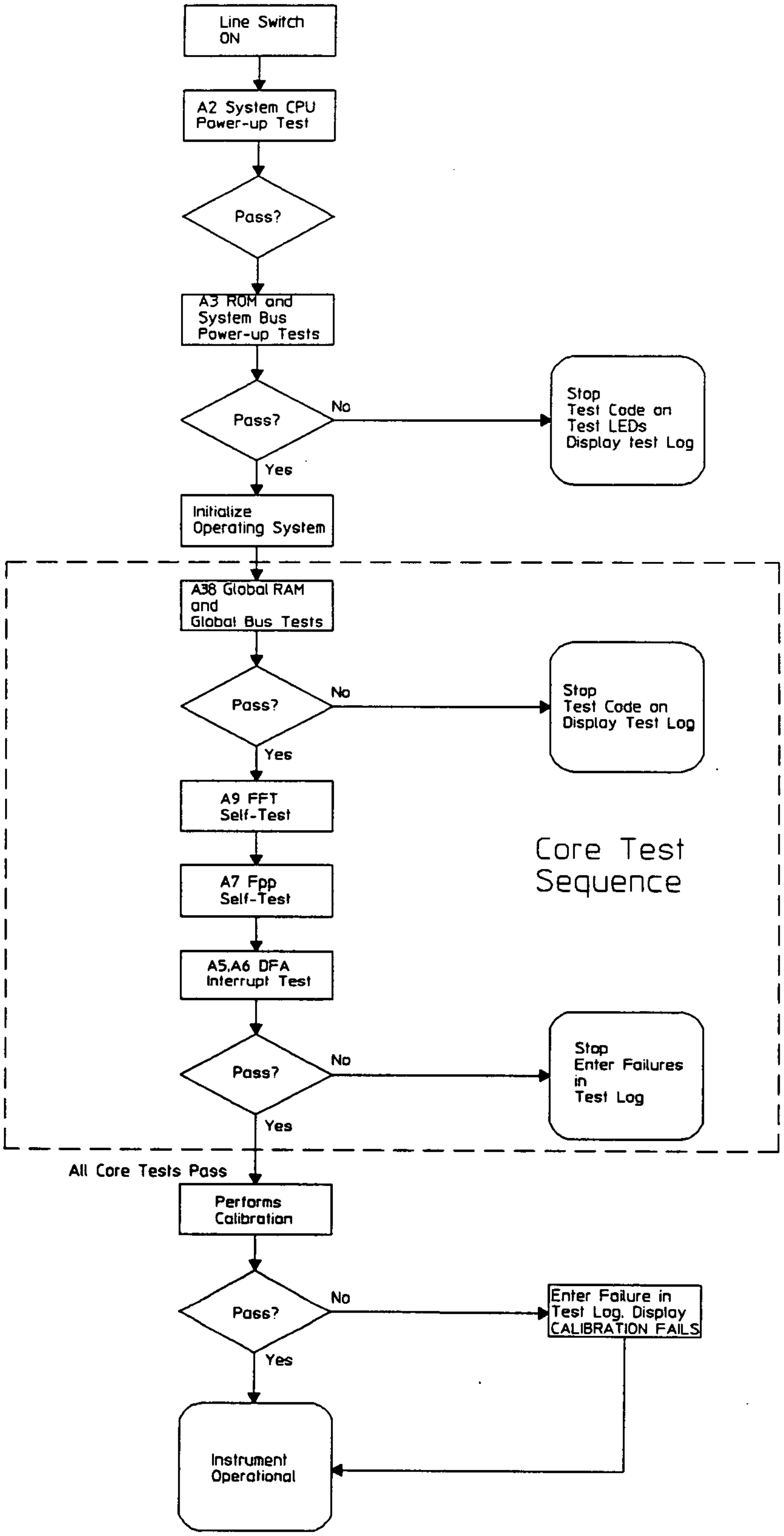

Line Switch ON
A2 System CPU Power-up Test
Pass?
A3 ROM and System Bus Power-up Tests
Pass?
No
Stop Test Code on Test LEDs Display test Log
Yes
Initialize Operating System
A38 Global RAM and Global Bus Tests
Pass?
No
Stop Test Code on Display Test Log
Yes
A9 FFT Self-Test
A7 Fpp Self-Test
A5,A6 DFA Interrupt Test
Core Test Sequence
Pass?
No
Stop Enter Failures in Test Log
Yes
All Core Tests Pass
Performs Calibration
Pass?
No
Enter Failure in Test Log, Display CALIBRATION FAILS
Yes
Instrument Operational

Figure 7-17. Power-Up Sequence Flowchart

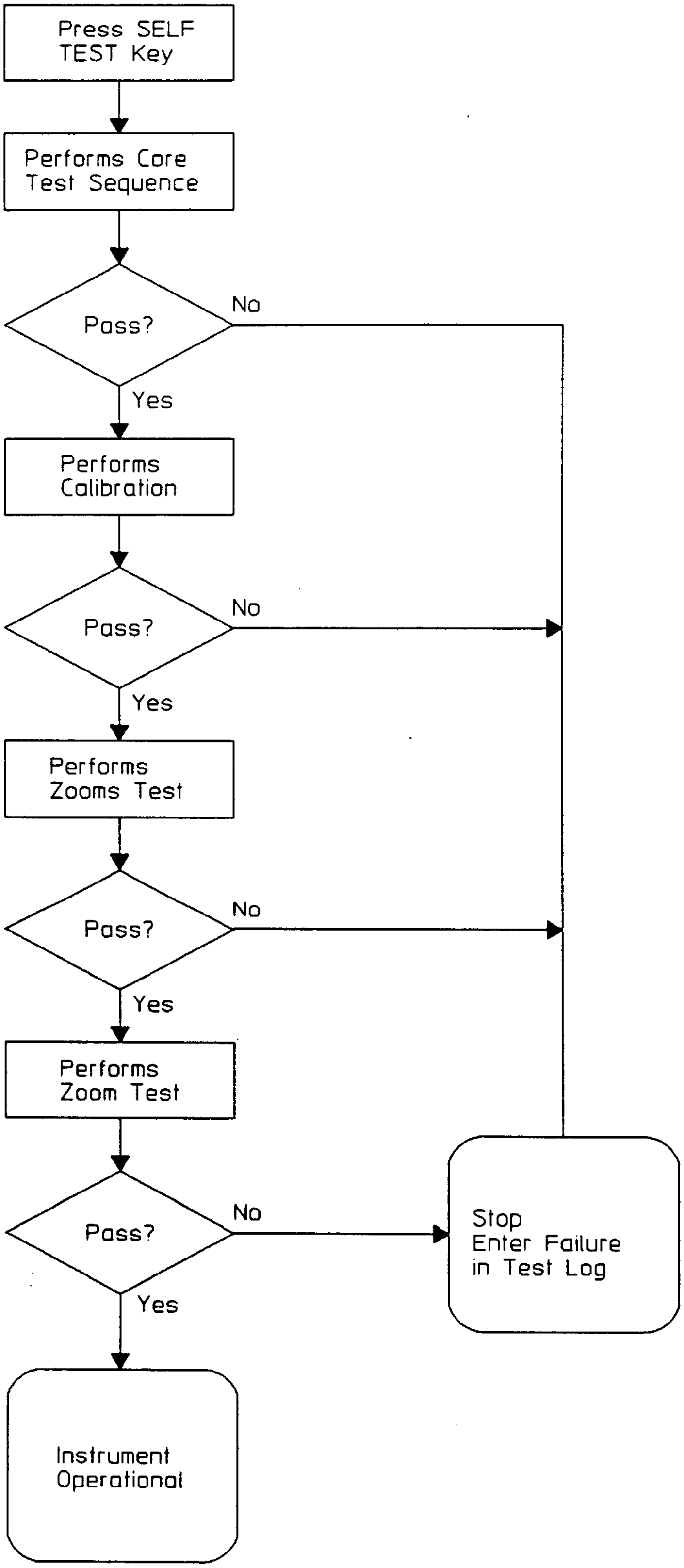


Figure 7-18. Self Test Sequence Flowchart

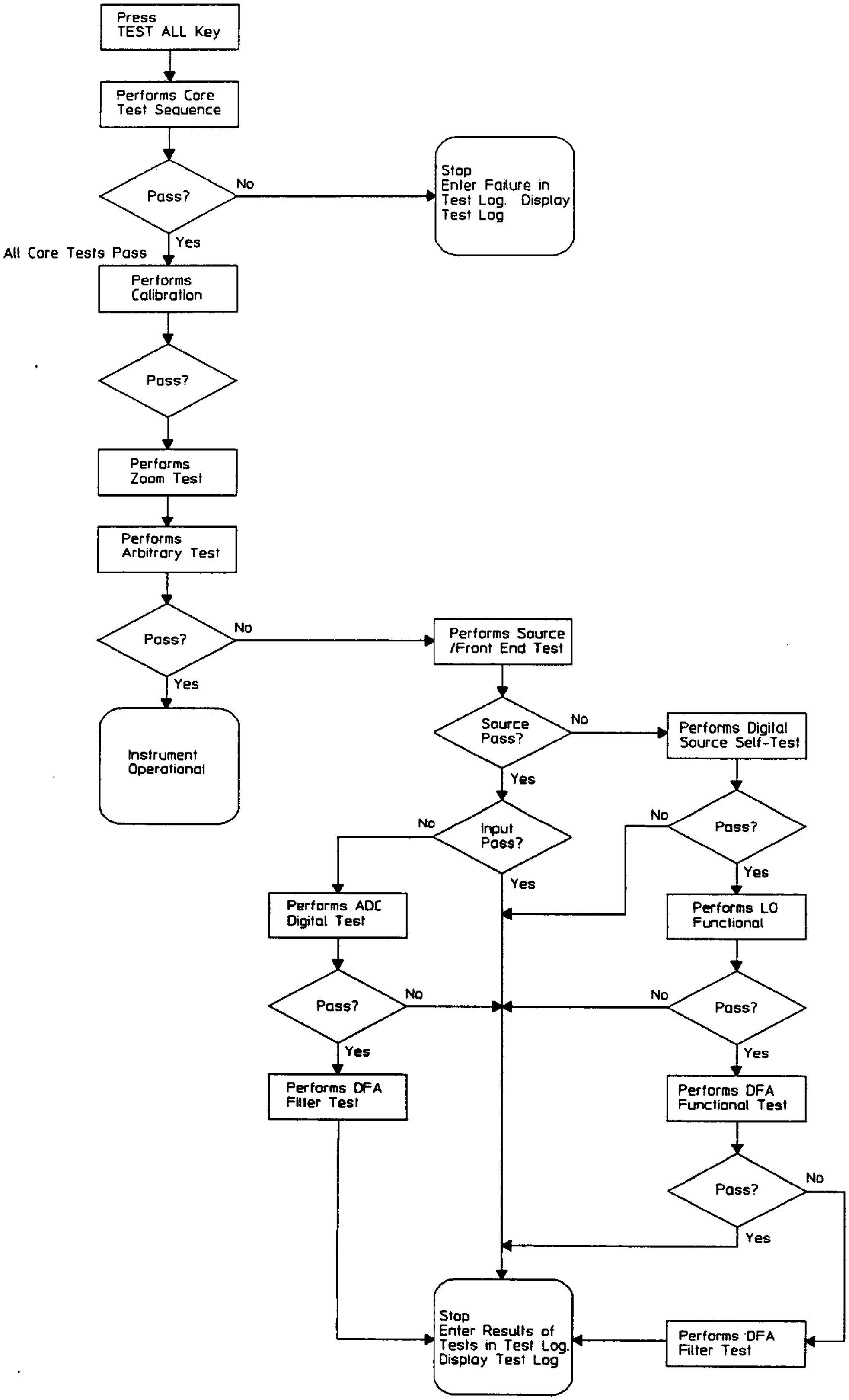


Figure 7-19. Test All Sequence Flowchart

SERVIC TEST

This softkey displays the first level of softkeys used in servicing the HP 3563A.

TEST ALL

The TEST ALL key invokes a sequence of self-tests that thoroughly exercises the digital and the analog hardware in the instrument. Each of the self-tests in the TEST ALL sequence can be run individually to help isolate the failure (Refer to the "Test All" discussion earlier in this section.) As the TEST ALL sequence is executed the results of each self-test is entered in the test log. When the sequence is completed the test log is displayed. Refer to figure 7-14 for the TEST ALL sequence.

TEST MEMORY

This key displays the menu of softkeys used in testing the Global RAM section of the A38 Memory and the A17 Display Interface.

GLOBAL RAM

This key initiates the global functional test (this test is done on power-up). The global bus is tested by echoing data over the bus. If this test passes, a "marching pattern" test is done to TEST ALL of the Global memory. In the marching pattern test, data is written into each memory location and then read from the memory location. The global RAM test also isolates problems on the address lines and in the refresh circuits. To find address failures, the memory is initialized by writing the address of each location into the location. The contents are then read out and verified.

PROG ROM

At this time, this test has no function. A complete test of the Program ROM is done on power-up.

DSPINT TEST 1, DSPINT TEST 2, DSPINT TEST 3, DSPINT TEST 4

These keys are used to isolated failures in the display interface circuits on the A38 Memory and A17 Display Interface assemblies. When one of these keys is pressed the display is disabled.

TEST PROC

This key displays the menu of softkeys used to test processing assemblies in the instrument.

TEST FPP

This key displays the menu of soft keys used to test the A7 Floating Point Processor. When a test is initiated, the A2 System CPU loads test data and FPP instructions into the global RAM section of the A38 Memory (except in the Reset FPP test) and commands the FPP to perform the test. After completing the test, the FPP sends the test results to global RAM and an interrupt (IRQT3L) to the system CPU. Any failed bits and the status of the interrupt are annunciated on the display. The "JUMPER ECHO" test requires jumper A7 J2B to be in the test position.

TEST FFT

This key displays the menu of softkeys used to test the A9 Fast Fourier Transform Processor. The FFT function test exercises the FFT functions by performing a forward and a reverse FFT, and exponential, Hanning, uniform, flattop, and user-defined windows on a known block of data. For a complete description of the FFT self-tests refer to "FFT Diagnostics" in Section VIII. The instrument needs to be preset before running any of the FFT self-tests. Several measurement setups can cause the FFT self-tests to fail by setting parameters used by the FFT to unknown values.

TEST DFA

This key displays the menu of softkeys used to test the A5 Digital Filter and the A6 Digital Filter Controller. The DFA functional test performs a zoom test using each channel on an internally generated square wave. This test does not use the inputs, ADCs, or analog source assemblies. The DFA PATT 1 test requires jumper A5 J7 to be set to test position. The DFA PATT 1 test is used for self-test and for signature analysis. The DFA PATT 2 is used only for signature analysis. When DFA PATT 2 is pressed "System Fault" is displayed.

TEST KEYBD

This key tests the A15 Keyboard system interface circuits. The A2 System CPU reads the keyboard status register and compares the result with a known good value. At the same time, the front panel LEDs are flashed on, then off.

TEST CPU

This key displays the menu of the softkeys used to test the HP-IB circuits on the A2 System CPU and the A22 HP-Interface Bus. The HP-IB FUNCTN key tests the General Purpose Interface Bus Adapter (A2 U412) by writing data to its registers and reading the data back. This test does not disturb devices connected to the HP-IB connector. The HP-IB DIAG key tests all of the HP-IB circuits and must not be run with devices attached to the HP-IB connector. The HP-IB CONNEC test is used to troubleshoot the A22 HP-IB connector. Refer to the "HP-IB Test" in the A2, A22 troubleshooting procedures in Section VIII for instructions.

TEST SOURCE

This key displays the menu of softkeys used in testing the A1 Digital Source, A4 Local Oscillator, and the A30 Analog Source.

SOURCE FUNCTN

The SOURCE FUNCTN key is used to test the A30 Analog Source (including the calibrator), the A32, A34 ADCs, and the A33, A35 Inputs. This test enables the analog source output and then the calibrator output into the input channels. The results are compared to known values. This test is the same test as the front end functional test(FR END FUNCTN).

FR END INTFCE

This key initiates the "Front End Interface" test (A1 Digital Source Diagnostics). The A2 System CPU loads the A1 Digital Source with test data for the front end interface circuits (control registers subblock). The system CPU then reads the contents of the digital source's status registers. Failed bits of the status registers are entered in the test log. The front end interface test verifies the circuits on the digital source used to set up the A30 Analog Source, A31 Trigger, A32, A34 ADCs, and the A33, Input assemblies. Refer to the A1 troubleshooting procedures in Section VIII.

SOURCE MAIN

This key initiates the Digital Source Self-test. The A2 System CPU loads the A1 Digital Source with test data to test most of the digital source's subblocks. The system CPU then reads the contents of the digital source's status registers. Failed bits of the status registers are entered in the test log. (Refer to the A1 troubleshooting procedures in Section VIII.)

ARBITRARY

This key initiates the four Arbitrary Source Tests. Known arbitrary waveforms are sent from the A10 Digital I/O to Channel 1. The test uses the filtered channel of the A5 Digital Filter board at 100 kHz. The address counters and pre-scaler are verified. The Zeros Test and Ones Test change a bit, perform 16 measurements then verify the bit for accuracy.

ZOOM

This key initiates the Zoom Test. A zoomed measurement is done using a test signal from the A30 Analog Source. If this test passes, the A30 Analog Source main output, A4 LO, A5 Digital Filter, A6 Digital Filter Controller, A7 FPP, A9 FFT, and the A38 Global RAM are verified.

LO

This key displays the menu of softkeys used in testing the Local Oscillator.

LO FUNCTN

This key initiates the LO Functional test. This test causes the LO to output phase and sine values to the A2 System CPU. The system CPU then compares the values to known good values. This test first executes using external clocks (SYNC2 and 10 MHz) and then runs again substituting internal clocks for the SYNC2 and 10 MHz clocks.

LO DSA PATT 1

This key is used in the A4 Local Oscillator signature analysis tests.

LO DSA PATT2

This key is used in the A4 Local Oscillator signature analysis tests.

TEST INPUT

This key displays the menu of softkeys used in testing and adjusting the A30 Analog Source, A32, A34 Analog Digital Converter and the A33, A35 Input assemblies.

FR END ADJUST

This key displays the menu of softkeys used in adjusting the instrument. For a complete description of the adjustments, refer to Section III, "Adjustments".

ADC

This key displays the menu of softkeys used in testing the A32, A34 Analog Digital Converter. The A5 Digital Filter status words are displayed when DIGTAL TRACE, PASS THRU, or SECOND PASS keys are pressed.

FR END FUNCTN

The FR END FUNCTN key is used to test the A30 Analog Source (including the calibrator), the A32, A34 ADCs, and the A33, A35 Inputs. This test enables the analog source output and then the calibrator output into the input channels. The results are compared to known values. This test is the same test as the Source Test (SOURCE FUNCTN).

FIRST PASS

This key displays the result of the first conversion pass of the ADCs. Refer to the A32, A34 troubleshooting procedures in Section VIII.

DIGTAL TEST

This key initiates a test of the ADC's digital section. The ADC Controller (A32 U602) outputs test patterns to the A5 Digital Filter. The A2 System CPU reads the results from the A5 Digital Filter and compares the results with known good values.

DIGTAL TRACE

When this key is pressed, a test pattern is generated. By running the Digital Trace test in loop mode, a logic probe or oscilloscope can be used to trace digital signals on the A32, A34 assemblies.

PASS THRU

When this key is pressed, the ADC's outputs are displayed in the test log.

SECOND PASS

This key displays the result of the second conversion pass of the ADCs. Refer to the A32, A34 troubleshooting procedures in Section VIII.

DIGTAL

This key displays the menu of softkeys used in testing the A1 Digital Source, the A5 Digital Filter and the A10 Digital I/O board.

INTERN PATH

This key tests the internal path from the A1 Digital Source board to Channel 1. The A1 Digital Source, the A5 Digital Filter and the A10 Digital I/O are verified.

EXTERN POD 1

This key tests the external pod cable connections to Channel 1. This test requires external hookup with the A40 Test Board. The A10 Digital I/O and the A5 Digital Filter board are verified.

EXTERN POD 2

This key tests the external pod cable connections to Channel 2. This test requires external hookup with the A40 Test Board. The A10 Digital I/O and the A5 Digital Filter board are verified.

QUALFR POD

This key tests the external qualifier pod cable connections. This test requires external hookup with the A40 Test Board. The A10 Digital I/O and the A5 Digital Filter board are verified.

TEST RESULT

This key displays the menu for the Test Log and the Fault Log. (Refer to the "Test Log and Fault Log Descriptions"in this section for a detailed description. The CLEAR TEST key is used to clear the Test Log (press twice to clear log). The CLEAR FAULT key is used to clear the Fault Log (press twice to clear log).

LOOP ON OFF

This key activates and disables the loop mode. The loop mode is used for signature analysis tests and to find intermittent failures. Refer to "Loop Mode and Intermittent Failures" in this section for a complete description of the loop mode and how to use it.

Self-Calibration

The HP 3563A has a stable internal calibration source which is used periodically to calibrate the input circuits. The calibration signal is generated on the A30 Analog Source circuit board. The self-calibration runs at the following times if the 'AUTO' calibration key is on: power-on, 8 minutes after power-on, 12 minutes after power-on, 40 minutes after power-on, and every two hours thereafter.

The self-calibration process consists of taking various measurements then generating calibration curves. These curves are used to correct measurements before they are displayed (the A7 FPP includes in its measurement process a complex multiply by a calibration correction curve). Since the calibration adjustments are done to the measurement after it is taken, the input assemblies remain unchanged by the calibration process (except for the value put in the common mode rejection DAC, refer to Section VI, "A5 Digital Filter" for a description of the common mode rejection DAC). The following measurements are taken to produce the calibration curves:

- Free-run measurement using the fixed sine from the analog source. This measurement is used to set the common mode rejection DAC on the A33, A35 Input assemblies.
- Single channel triggered measurements using the calibrator; Pseudo Random Noise Source subblock (PRN), the inverse of the PRN, and the 64 kHz square wave.
- Free-run frequency response measurement using the periodic chirp from the analog source
- Free-run measurement using the fixed sine from the analog source.

Displaying Calibration Curves

1. Press the HP 3563A keys as follows to display an example of the calibration curves:

⌈ Control ⌉
PRESET ..... RESET

⌈ Input Setup ⌉
RANGE ..... 0 dBVrms

⌈ Measurement ⌉
WINDOW ..... UNIFRM
(NONE)

⌈ Display ⌉
A&B

⌈ Control ⌉
PAUSE/CONT

⌈ Control ⌉
SPCL
FCTN ...... BEEPER
ON OFF – **516** ..... ENTER
(toggle key)

⌈ Display ⌉
SCALE ..... Y FIXD
SCALE ..... – **1.5, 1.5** dB

Refer to figure 7-20 to see the example of the calibration curves. The range and source level can be varied to display calibration curves for different ranges.

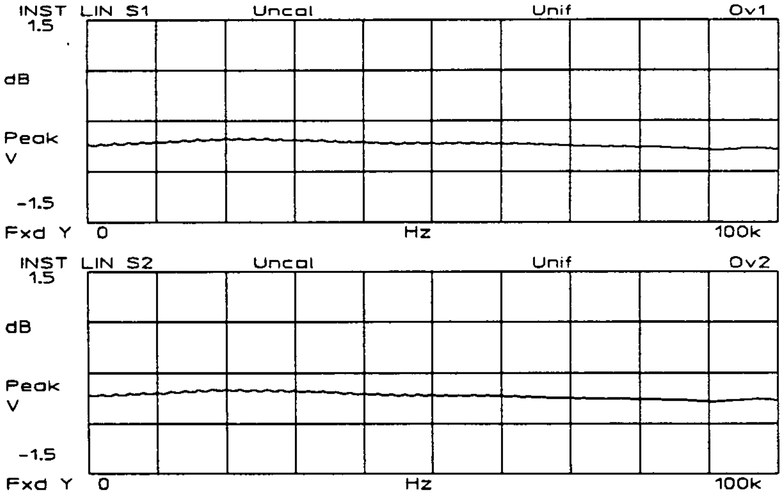


Figure 7-20. Calibration Curves

Calibration Failures

Introduction

There are three type of calibration failures:

- Calibration Wait
- Calibration Accuracy
- Calibration Source

Calibration failure messages are entered in the test log on power-up and when self-test or "Test All" are run. A calibration wait failure means the calibration measurement did not complete within the specified time. A calibration accuracy failure means the magnitude or phase values exceeded the following calibration limits:

Single Channel Flatness
± 1.5 dBVpk,

Frequency Response
± 30 dBVpk, ± 40°

Single Channel Phase at 0°
± 1.5°

If the calibration accuracy failure occurs, the failure is entered in the test log and the calibration curves are used in measurement reading. Any assembly in the instrument can cause a calibration failure. If calibration fails, run the "Test All" diagnostic to isolate the failing assembly (presented earlier in this section). It is also possible that all the assemblies pass their self-tests and there still is a calibration failure.

If the assemblies self-tests pass except for a "Calibration Wait" failure, the measurement may not be triggering. Verify the trigger circuits in the instrument. See "Isolating Trigger Failures" earlier in this section.

If the assemblies self-tests pass except for a "Calibration Accuracy" failure, the following may be occurring:

1. The A30 Analog Source, A31 Trigger, A32, A34 ADCs, or the A33, A35 Input assemblies need adjustment (refer to Section III).
2. The A30 Analog Source, A31 Trigger, A32, A34 ADCs, or the A33, A35 Input assemblies are failing. Follow the "Isolating Front End Failures" procedure (earlier in this section) and look for amplitude variations.

If the assemblies self-tests pass except for a "Calibration Source' failure, check the instrument's trigger circuits (refer to "Isolating Trigger Failures") and the Pseudo Random Noise Source subblock on the A30 Analog Source.

Calibration Failure Tests

1. Only a few ranges and Channel 2 are used for calibration amplitude measurements (frequency response measurements are done using Channel 1 and Channel 2). The calibration curves for Channel 1 and the ranges not directly measured are calculated using the measured data. The ranges used in the measured data are as follows:

   1, 8, 0, −1, −12, −13 dBVrms

   To check these ranges, use the "Displaying Calibration Curves" procedure.
2. To disable the calibrator, toggle the line switch then press softkey S8 (the last softkey) just after the display appears. The input channels can now be verified without using the calibrator. Input a source into Channel 1 and Channel 2. The waveforms now displayed are not corrected with the calibration curves.
3. To verify the calibrator is operating correctly, pull up A32, A33, A34, and A35 in their card nests. Perform the "Calibration Circuits Test" in Section VIII.

Troubleshooting the Auto-Range Circuits

This procedure assumes Test All passes. Refer to the "Test All" procedures earlier in this section.

Note The HP 3563A has differential inputs. If the inputs are not terminated and a low range is set, the over range LEDs may be on. Some instruments are more sensitive to external noise than others.

Symptoms

1. The instrument measures correctly when the range is set (auto-range is off).
2. An over range LED stays on when the instrument is at the correct range and measuring correctly.

These failures can be caused by one of the following conditions:

- An over range or half scale circuit in the input(A33, A35), ADC (A32, A34), or the digital filter (A5) assemblies is defective.
- There is noise in the input channels. The calibrator can correct for a small amount of noise. However, when operating the inputs at full scale at a low range, noise can cause the over range LEDs to come on.
- The LEDs are failing. If this is suspected, perform the "Keyboard Check" procedure in the "Initial Conditions Test".

Auto-Range Failure Tests

Auto-Range Failure Test ONE

Determines if the over-range, half-range circuits are functioning correctly.

1. Input a 2 Vrms, 1 kHz sine wave to both channels.
2. Press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

[Input Setup]
RANGE ...... 3 Vrms

[Control]
SPCL
FCTN ...... SERVICE TEST ...... LOOP ON OFF

...... TEST INPUT ...... ADC

...... DIGTAL TRACE

The half-range LED should be on and the digital filter status Word for both channels should be 01 (MSB is to the left, ignore leading zeros).

3. Increase the input level to **3** Vrms. Both the over-range and half-range LEDs should be on and the digital filter status words should binary 00011.
4. Decrease the input level to **0.5** Vrms. The over-range and half-range LEDs should be off and the digital filter status words should be 0.
5. If this test fails, perform "Auto-Range Failure Test THREE."

If this test passes, the over-range and half-scale circuits are most likely operating correctly; perform "Auto-Range Failure Test TWO".

Auto-Range Failure Test TWO

Determines if the over-range, half-range problem is range related or caused by noise. The test inputs a sine wave at different voltage levels and sets the range for the sine wave level. Refer to table 6- for a chart of all possible ranges. The test starts with the – 51 dBVrms (2.82 mVrms) range.

1. Press the line switch OFF and remove the top cover.
2. Press the line switch ON.
3. Input a 2.8 mVrms, 1 kHz sine wave to the failing channel.
4. Press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

[Input Setup]
RANGE ...... **2.82** mVrms

5. Using an oscilloscope, look at the waveform at A32 (or A34) TP100.

If the signal is noise or distorted, troubleshoot the input (A33, A35) and ADC assemblies (A32, A34). Start with "Isolating Front End Failures Procedure Five — Input, ADC, and Digital I/O Failures".

If the –51 dBVrms range is okay, verify ranges –36 dBVrms (15.8 mVrms), –5 dBVrms (0.5623 Vrms), 0 dBVrms (1 Vrms), and 9 dBVrms (2.818 Vrms). If the problem has not been isolated, continue with "Auto-Range Failure Test THREE".

Auto-Range Failure Test THREE

Determines if the problem is in the input section or the digital section of the instrument.

1. Press the line switch OFF, remove the top cover and the digital board retainer bar.
2. Place the A5 Digital Filter assembly on the extender board.
3. Terminate both input channels by using two 50 Ω feedthrough terminations and ground the BNC shells as shown in figure 7-21.

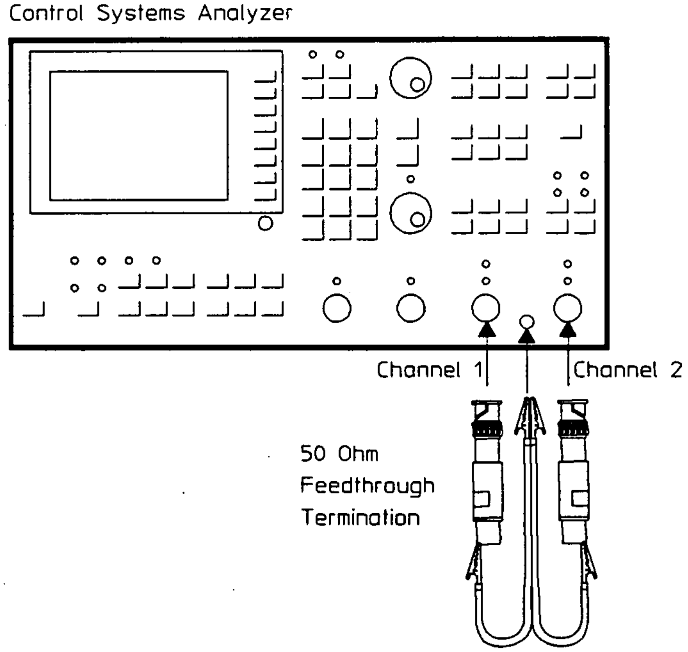


Figure 7-21. Auto-Range Failure Test Three Setup

4. Press the HP 3563A keys as follows:

```
[ Control ]
  PRESET      ......     RESET

[ Control ]
  SPCL
  FCTN        ......     SERVICE
                         TEST        ......    LOOP
                                               ON OFF
              ...... TEST
                     INPUT           ......    ADC
                                     ......    DIGTAL
                                               TRACE
```

5. Note the value of the digital filter status word for each channel. The values should be 0.

   The over-range and half-range LEDs should be off. If the instrument is not failing at the – 51 dBVrms range, set the instrument to the failing range.

6. Check A5 U306 pins 2, 4, 11, and 13. Each of these signals should be TTL level low. If any of the signals are TTL level high or a changing value, troubleshoot the input (A33, A35) and ADC assemblies (A32, A34). Start with "Isolating Front End Failures Procedure FIVE — Input, ADC, and Digital I/O Failures".
7. Press the line switch off and set jumpers A5 J2 and A5 J3 in test (T) position.
8. Press the line switch on. A system fault occurs with these jumpers in test position.
9. Repeat step 4.
10. If the digital filter status words changed or the failure moved from one channel to the other channel, troubleshoot the input(A33, A35) and ADC assemblies (A32, A34). Start with "Isolating Front End Failures Procedure FIVE — Input, ADC, and Digital I/O Failures".
11. If the digital filter status words remain the same, the most likely cause of the failure is the A5 Digital Filter Assembly.

Section VIII

Table of Contents

Section VIII: Service

Section VIII

Service

Introduction

This section contains all the information required to isolate failures to the component level. Use this section after using the fault isolation procedures in Section VII. This section is used to isolate a failure to the subblock level. Each functional subblock consists of a small number of components, and the technician's expertise is relied upon to isolate the faulty component.

Caution Many of the parts are static sensitive. Use the appropriate precautions when removing, handling and installing all parts to avoid unneccessary damage.

How to Use This Section

Start

After isolating the fault to an assembly, go to the troubleshooting procedures for that assembly. The troubleshooting information is listed in order of the circuit board assembly number, A1 through A33.

Reference

Use the component locators and schematics which follow each of the troubleshooting procedures.

For the location of cables and boards refer to figure 4-1 in Section IV.

For the circuit block diagrams refer to Section VI.

To understand the instrument's operation and signal mnemonics refer to Section VI.

Keys

There are two types of keys on the HP 3563A, hardkeys and softkeys. Hardkeys are organized on the front panel according to functional group. See figure 8-1. In these procedures, the functional group is in brackets, the hardkeys appear in bold text, and the softkeys are in regular text.

For example:

[Measurement]
FREQ ...... FREQ
SPAN

[Entry]
1
0 ...... kHz

This example instructs you to first press the hardkey FREQ which is found in the Measurement group followed by the softkey FREQ SPAN. Next, enter the number 10 on the numeric keypad located in the Entry group. Specify the measurement unit by pressing the kHz softkey.

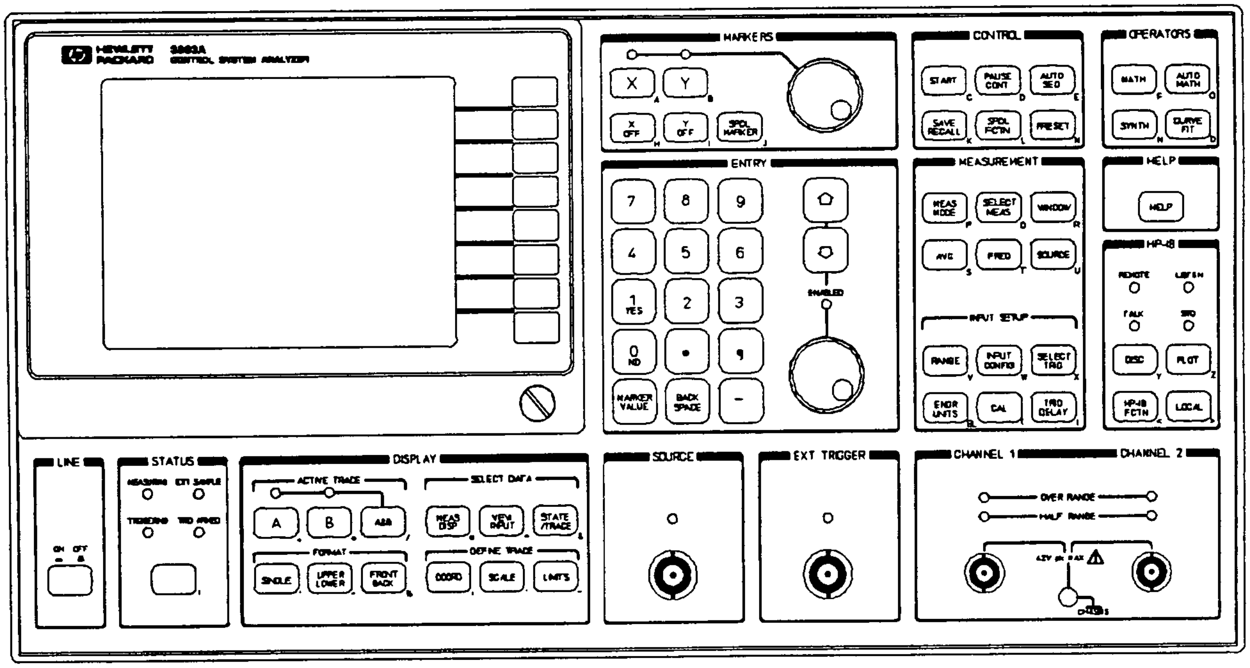


Figure 8-1. HP 3563A Front Panel Illustration

Note

In the following test procedures, numeric values may require multiple keystrokes. In the previous example, the value 10 requires two keystrokes, 1 and 0. In the procedures, these keystrokes are represented as 10.

If you make an incorrect keystroke, press the previous hardkey. This will return you to a first level menu which allows you to continue with the procedure.

Loop Mode

The loop mode is used for some signatures analysis tests and to find intermittent failures. For description of the loop mode refer to "Loop Mode and Intermittent Failures" in Section VII.

Note

After completing a test or repair, check that all jumpers are in the NORMAL or RUN position and that all cables are connected.

Recommended Test Equipment

The recommended test equipment for troubleshooting is listed in table 1-2. Any item which meets or exceeds the critical requirements can be substituted for the model listed.

Logic Conventions

Positive logic convention is used in this manual unless otherwise noted. Positive logic conventions define a logic "1" or "High" as more positive voltage and a logic "0" or "Low" as the more negative voltage.

Safety Considerations

The HP 3563A is a Safety Class 1 instrument (provided with a protective earth terminal). The instrument and manuals should be reviewed for safety markings and instructions before operation. Refer to the safety symbol table in the preface of this manual.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling and installing all parts to avoid unneccessary damage.

Warning

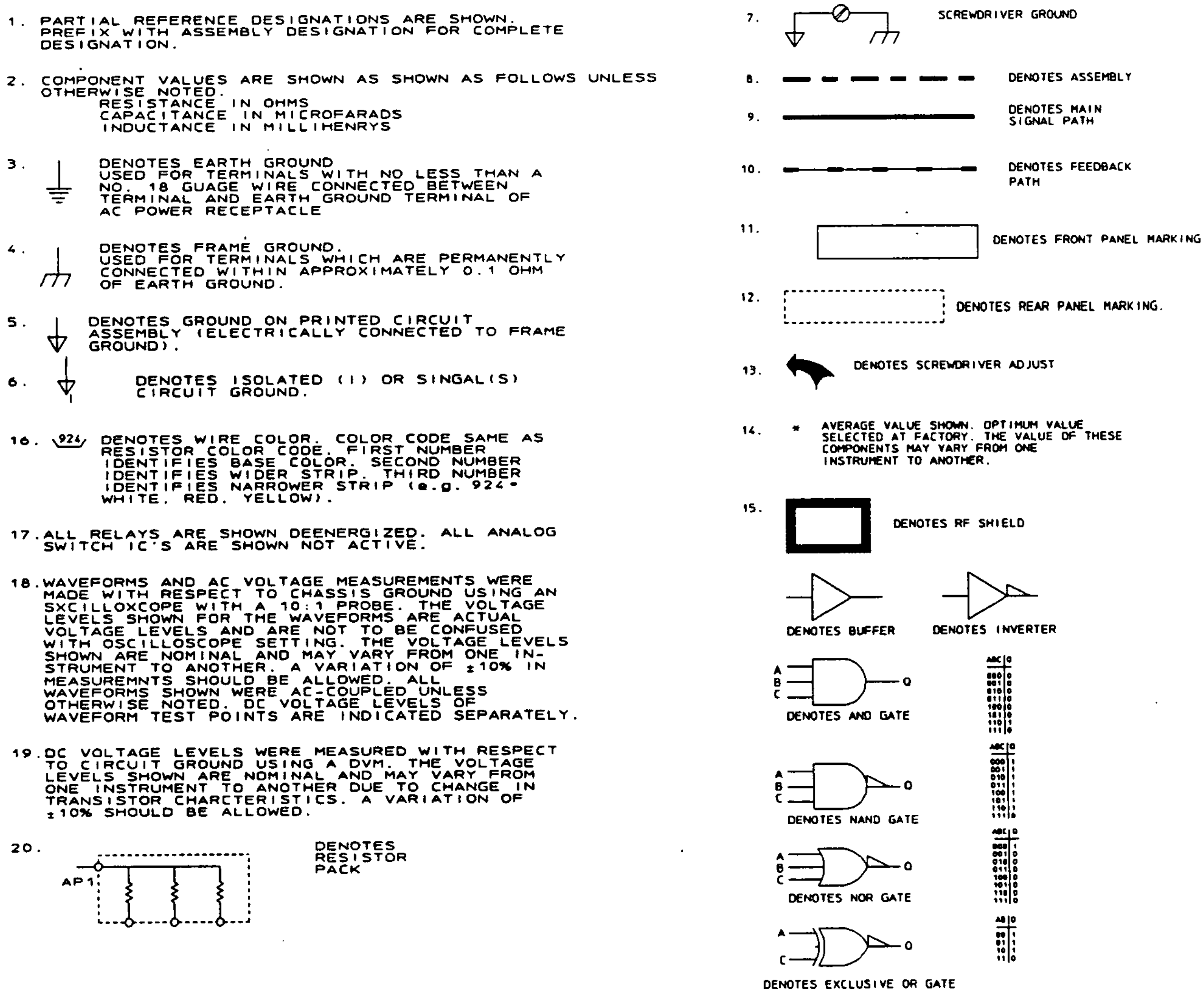
230 Vdc is present in the A18 power supply assembly even with the line switch in the off position and the power cord removed. Be extremely careful when working in the power supply area. This high voltage could cause serious personal injury if contacted. To discharge the capacitors holding this voltage perform steps 1 through 3.

1. **Remove the power cord from the rear panel.**
2. **Remove the bottom cover and power supply shield.**
3. **Wait two minutes after turning the power off to allow the capacitors to discharge.**

General Schematic Notes

Each troubleshooting section contains the assembly's schematic diagrams which show the detailed circuits of the HP 3563A. Each schematic is assigned a numerical callout (A1 through A35) which matches the assembly's mnemonic. Refer to table 8-3 for a description of the mnemonics. The overall block diagram for the instrument is shown in figure 8-2 at the end of this section.

Table 8-1. General Schematic Notes



1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY DESIGNATION FOR COMPLETE DESIGNATION.

2. COMPONENT VALUES ARE SHOWN AS SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
RESISTANCE IN OHMS
CAPACITANCE IN MICROFARADS
INDUCTANCE IN MILLIHENRYS

3. DENOTES EARTH GROUND USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GUAGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OF AC POWER RECEPTACLE

4. DENOTES FRAME GROUND. USED FOR TERMINALS WHICH ARE PERMANENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.

5. DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY (ELECTRICALLY CONNECTED TO FRAME GROUND).

6. DENOTES ISOLATED (I) OR SINGAL(S) CIRCUIT GROUND.

16. 924 DENOTES WIRE COLOR. COLOR CODE SAME AS RESISTOR COLOR CODE. FIRST NUMBER IDENTIFIES BASE COLOR. SECOND NUMBER IDENTIFIES WIDER STRIP. THIRD NUMBER IDENTIFIES NARROWER STRIP (e.g. 924= WHITE, RED, YELLOW).

17. ALL RELAYS ARE SHOWN DEENERGIZED. ALL ANALOG SWITCH IC'S ARE SHOWN NOT ACTIVE.

18. WAVEFORMS AND AC VOLTAGE MEASUREMENTS WERE MADE WITH RESPECT TO CHASSIS GROUND USING AN SXCILLOXCOPE WITH A 10:1 PROBE. THE VOLTAGE LEVELS SHOWN FOR THE WAVEFORMS ARE ACTUAL VOLTAGE LEVELS AND ARE NOT TO BE CONFUSED WITH OSCILLOSCOPE SETTING. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER. A VARIATION OF ±10% IN MEASUREMNTS SHOULD BE ALLOWED. ALL WAVEFORMS SHOWN WERE AC-COUPLED UNLESS OTHERWISE NOTED. DC VOLTAGE LEVELS OF WAVEFORM TEST POINTS ARE INDICATED SEPARATELY.

19. DC VOLTAGE LEVELS WERE MEASURED WITH RESPECT TO CIRCUIT GROUND USING A DVM. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER DUE TO CHANGE IN TRANSISTOR CHARCTERISTICS. A VARIATION OF ±10% SHOULD BE ALLOWED.

20. DENOTES RESISTOR PACK

7. SCREWDRIVER GROUND

8. DENOTES ASSEMBLY

9. DENOTES MAIN SIGNAL PATH

10. DENOTES FEEDBACK PATH

11. DENOTES FRONT PANEL MARKING

12. DENOTES REAR PANEL MARKING.

13. DENOTES SCREWDRIVER ADJUST

14. * AVERAGE VALUE SHOWN. OPTIMUM VALUE SELECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTRUMENT TO ANOTHER.

15. DENOTES RF SHIELD

DENOTES BUFFER

DENOTES INVERTER

DENOTES AND GATE

ABC	0
000	0
001	0
010	0
011	0
100	0
101	0
110	1
111	0

DENOTES NAND GATE

ABC	0
000	1
001	1
010	1
011	1
100	1
101	1
110	1
111	0

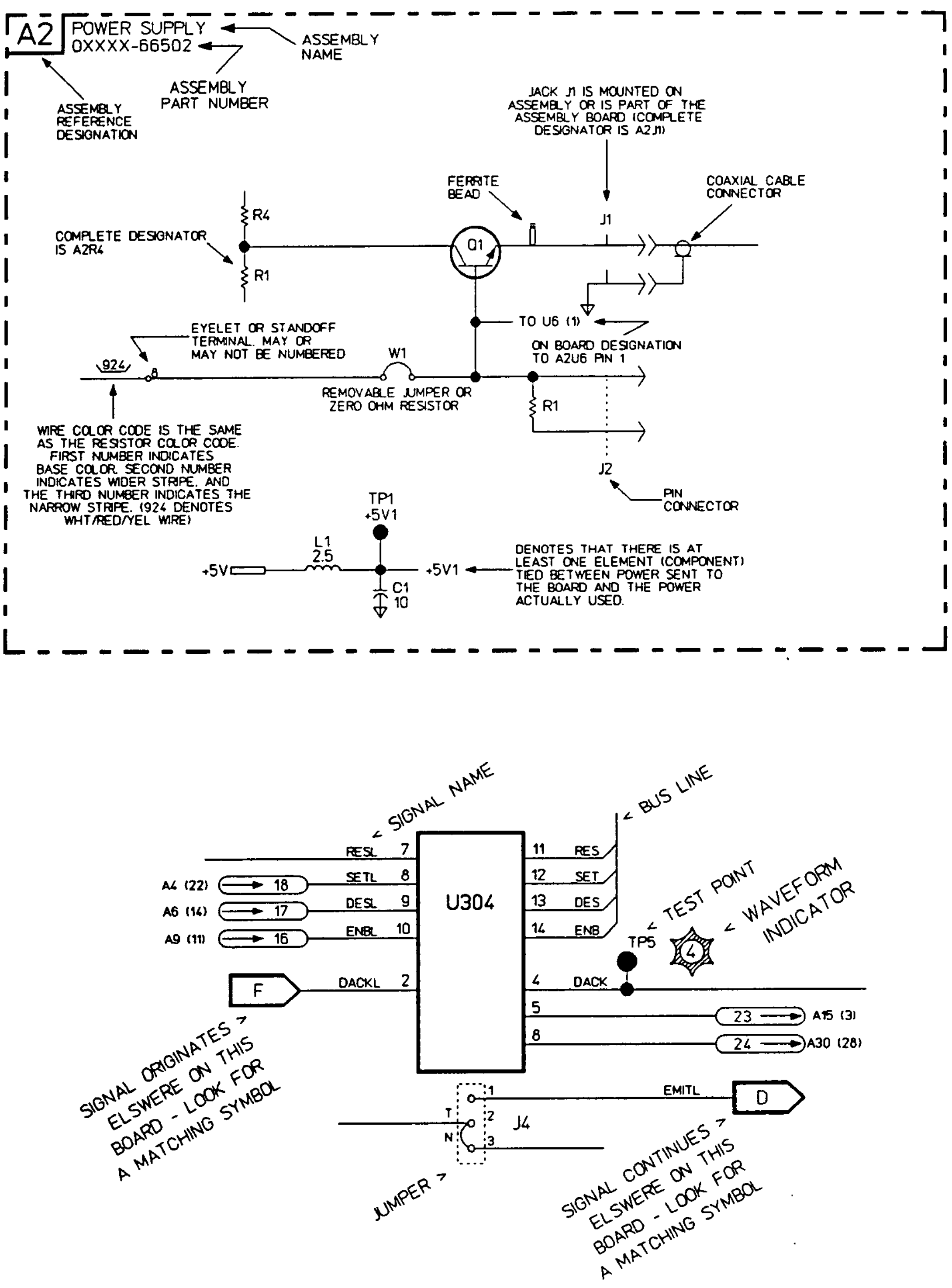
DENOTES NOR GATE

ABC	0
000	1
001	0
010	0
011	0
100	0
101	0
110	0
111	0

DENOTES EXCLUSIVE OR GATE

AB	0
00	1
01	1
10	1
11	0

Table 8-2. Reference Designators


A2
POWER SUPPLY
0XXXX-66502
ASSEMBLY NAME
ASSEMBLY PART NUMBER
ASSEMBLY REFERENCE DESIGNATION
JACK J1 IS MOUNTED ON ASSEMBLY OR IS PART OF THE ASSEMBLY BOARD (COMPLETE DESIGNATOR IS A2J1)
FERRITE BEAD
COAXIAL CABLE CONNECTOR
J1
R4
COMPLETE DESIGNATOR IS A2R4
Q1
R1
EYELET OR STANDOFF TERMINAL. MAY OR MAY NOT BE NUMBERED
924
8
W1
TO U6 (1)
ON BOARD DESIGNATION TO A2U6 PIN 1
REMOVABLE JUMPER OR ZERO OHM RESISTOR
R1
J2
PIN CONNECTOR
WIRE COLOR CODE IS THE SAME AS THE RESISTOR COLOR CODE. FIRST NUMBER INDICATES BASE COLOR. SECOND NUMBER INDICATES WIDER STRIPE. AND THE THIRD NUMBER INDICATES THE NARROW STRIPE. (924 DENOTES WHT/RED/YEL WIRE)
TP1
+5V1
L1
2.5
+5V
+5V1
C1
10
DENOTES THAT THERE IS AT LEAST ONE ELEMENT (COMPONENT) TIED BETWEEN POWER SENT TO THE BOARD AND THE POWER ACTUALLY USED.
< SIGNAL NAME
< BUS LINE
RESL 7
SETL 8
DESL 9
ENBL 10
DACKL 2
U304
11 RES
12 SET
13 DES
14 ENB
4 DACK
5
8
A4 (22) 18
A6 (14) 17
A9 (11) 16
F
< TEST POINT
TP5
4
< WAVEFORM INDICATOR
23 A15 (3)
24 A30 (28)
SIGNAL ORIGINATES ELSWERE ON THIS BOARD - LOOK FOR A MATCHING SYMBOL >
EMITL
D
T
N
1
2
3
J4
JUMPER >
SIGNAL CONTINUES ELSWERE ON THIS BOARD - LOOK FOR A MATCHING SYMBOL >

NOTE: THE ⊂⊃ SYMBOL INDICATES A PIN OF THE EDGE CONNECTOR WHICH PLUGS INTO THE MOTHER BOARD.

EXAMPLE: GRAMRSTL (12 →) A8 (119)

PIN 12 OF THE EDGE CONNECTOR ON THIS BOARD CARRIES THE SIGNAL GRAMRSTL TO PIN 119 OF THE EDGE CONNECTOR OF THE A8 BOARD VIA THE MOTHER BOARD.

Table 8-3. Assembly Mnemonics

Mnemonics	Description
A1 DGTL SCE	Digital Source
A2 CPU/HP-IB	System CPU/HP-IB
A4 LO	Local Oscillator
A5 DGTL FLTR	Digital Filter
A6 D FLTR CONT	Digital Filter Controller
A7 FPP	Floating Point Processor
A9 FFT	Fast Fourier Transform Processor
A14 MOTHERBD	Mother Board
A15 KEYBD	Keyboard
A17 DSPL	Display Interface
A18 PWR SPLY	Power Supply
A20 CONN BRD 1	Digital Connector Board
A21 CONN BRD 2	Digital Connector Board
A22 HP-IB	HP-Interface Bus
A30 ANLG SCE	Analog Source
A31 TRIG	Trigger
A32 ADC 1	Analog Digital Converter, Channel 1
A33 INPUT 1	Input Channel 1
A34 ADC 2	Analog Digital Converter, Channel 2
A35 INPUT 2	Input Channel 2
A38 MEM	Memory Board
A40 TEST BRD	Digital Test Board
A41 ANLG EXT	Analog Extender Board
A42 INPUT EXT	Input/Analog Extender Board

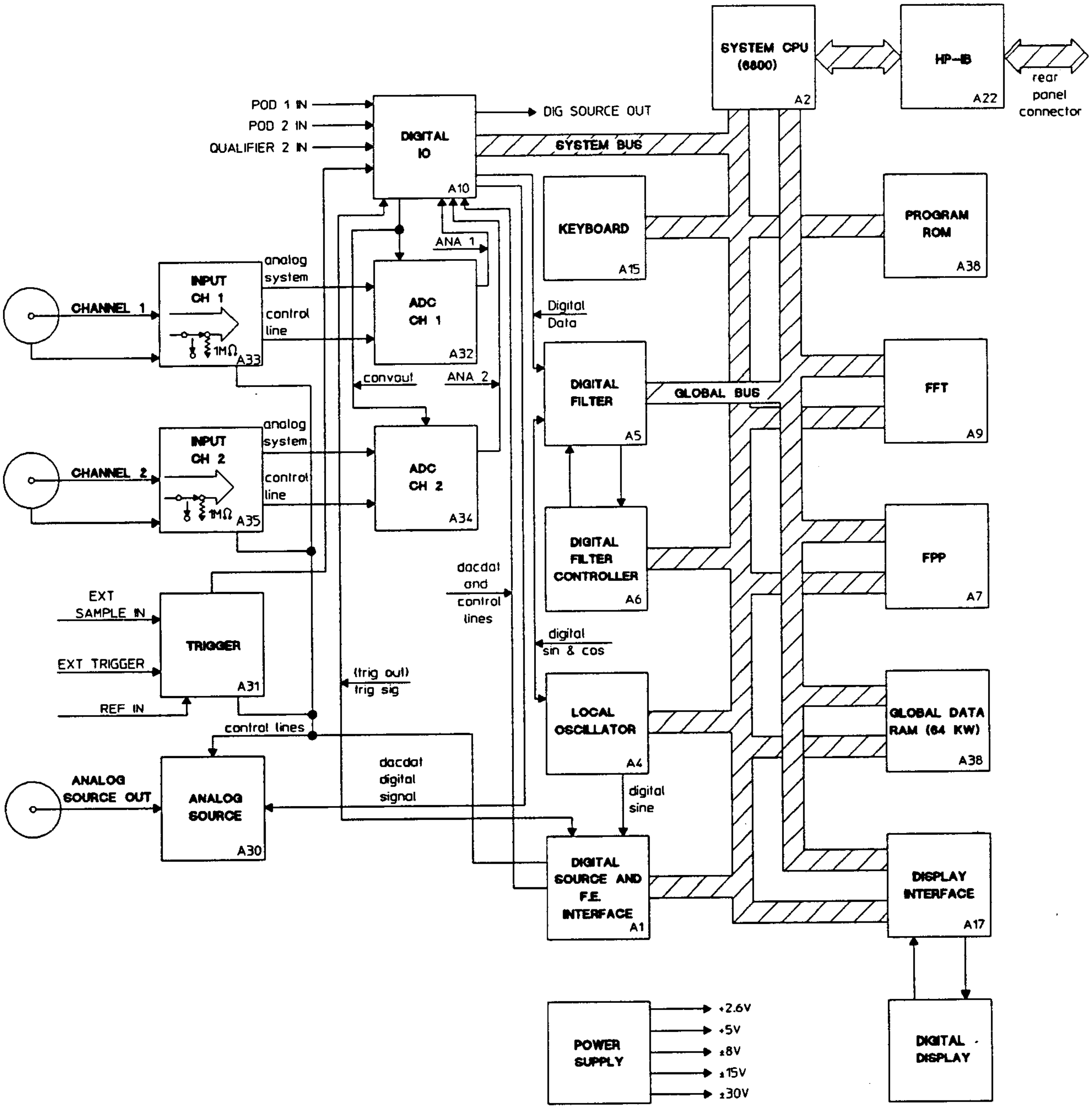


Figure 8-2. HP 3563A Block Diagram

A1
Digital Source

A1 Digital Source

The information in this section should be used to isolate faulty subblocks in the A1 Digital Source assembly. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the circuit descriptions of Section VI are understood.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Caution Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	The primary method for troubleshooting the digital source assembly is to use signature analysis and the waveforms provided in the "Digital Source Signature Analysis Tests" and the "Digital Source Waveforms" sections which follow. Start troubleshooting by using the "Digital Source Diagnostics" procedures to isolate the failure to a subblock.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
Verify	Use the oscilloscope waveforms in table 8-13 to see correct operation at various test points in the assembly.
After-Repair	Use table 8-14 to determine which adjustments and tests need to be done to complete instrument service.

Digital Source Diagnostics

The digital source is tested using two self-tests; the front end interface test and the source main test. When either of these tests are initiated, the test registers and control registers are loaded with test data and the TEST signal to the test registers goes low. The test is performed and the contents of the status registers is read and verified by the A2 System CPU. Any failed bits are annunciated on the display. These tests are also used in loop mode for signature analysis patterns.

1. To perform the self-tests, press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN      ......   SERVIC
                     TEST      ......   TEST
                                        SOURCE   .....   FR END
                                                         INTFCE

                                                 .....   SOURCE
                                                         MAIN
```

2. Refer to table 8-5 for single bit failures to determine the probable subblock failing.
3. Go to "Subblock Verification Tests" for multiple bit failures.
4. If both tests pass but a source function or a trigger mode is failing, use table 8-4 to determine the probable subblock failing.

Table 8-4. Digital Source Functions

Function Failing or Defective	Probable Cause of Failure
Triggered Mode	Phase Resolution Circuit (Go to "Digital Source Signature Analysis Tests")
Single Channel Phase	Phase Resolution Circuit (Go to "Digital Source Signature Analysis Tests")
CNTCLK	Control Registers (Go to "Digital Source Signature Analysis Test THREE")
Sine Wave Output	LO Input Receiver (Go to "Digital Source Signature Analysis Tests")
Source Energy Measurement fails (2-41) but random noise operates at full span	Effective Sample Rate Generator (Go to "Effective Sample Rate Generator Test")
Random Noise Output	Noise Generator (Go to "Digital Source Signature Analysis Test FOUR")
Burst Mode	Burst Control Circuit (Go to "Digital Source Signature Analysis Test FIVE")
SYNC OUT output	Burst Control Circuit (Refer to Waveform #5, Digital Source Waveforms)
Periodic Chirp	Effective Sample Rate Generator (Go to "Effective Sample Rate Generator Test")

Table 8-5. Digital Source Diagnostics

Bit #	Signal Name	From Component	Subblock Returning Status Bit Probable subblock failing
0	LDCH1L	U208-6	Control Registers (Go to "Digital Source Signature Analysis Test THREE")
1	LDCH2L	U208-7	
2	LDTRL	U208-5	
3	LDSRCL	U208-4	
4	SRCOUTFALTL	—	Status Registers (Go to "Digital Source Signature Analysis Tests")
5	UNLOCK	—	
6	C1OFSE	U101-7	Timing Control Circuit (Go to "Effective Sample Rate Generator Test")
7	CNTLD	U206-9	Control Registers (Go to "Digital Source Signature Analysis Test")
8	NCLK	U202-12	Burst Control Circuit (Go to "Digital Source Signature Analysis Test TWO")
9	DOUT	U209-6	Multiplier (Go to "Digital Source Signature Analysis Tests")
10	DMID	U13-13	LO Input Receiver (Go to "Digital Source Signature Analysis Tests")
11	NSR	U311-11	Noise Generator (Go to "Digital Source Signature Analysis Test FOUR")
12	CNTRL BUSY	U106-8	Control Registers (Go to "Digital Source Signature Analysis Test THREE")
13	BUSYL	U5-14	Phase Resolution Circuit (Go to "Digital Source Signature Analysis Tests")
14	TRIGGERED	U8-9	
15	ARMEDL	U5-15	
—	Digital Source Counters Fail	U305, U7,U107, U108	These counters are used in the following subblocks: Phase Resolution Circuit Timing Control Circuit Burst Control Circuit (Go to "Digital Source Signature Analysis Tests")

Subblock Verification Tests

The digital source performs several functions including generating band-limited random noise, interfacing the local oscillator with the analog source, synchronizing trigger operations, and interfacing the front end assemblies (inputs, ADCs, trigger, and analog source) with the A2 System CPU. Most functions use only a few of the DS subblocks. To isolate the failure to a subblock, use table 8-6 after performing the following steps:

1. Connect the front panel source output to Channel 1.
2. Connect the rear panel SYNC OUT output to Channel 2.
3. Press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

[Measurement]
RANGE ...... **5.6** V

[Measurement]
SOURCE ...... SOURCE LEVEL ...... **5** V
...... SOURCE TYPE ...... FIXED SINE ..... **1** kHz

[Display]
MEAS DISP ...... FILTRD INPUT ...... TIME REC1

[Display]
SCALE ...... Y FIXD SCALE ...... **6, −6** V

Refer to figure 8-3 to verify result.

Note

The free-run mode is used for most of the following waveforms. This is done to isolate failing functions to a subblock. When the trigger mode is not used, the waveforms move around on the display. The trigger mode is verified in step 7.

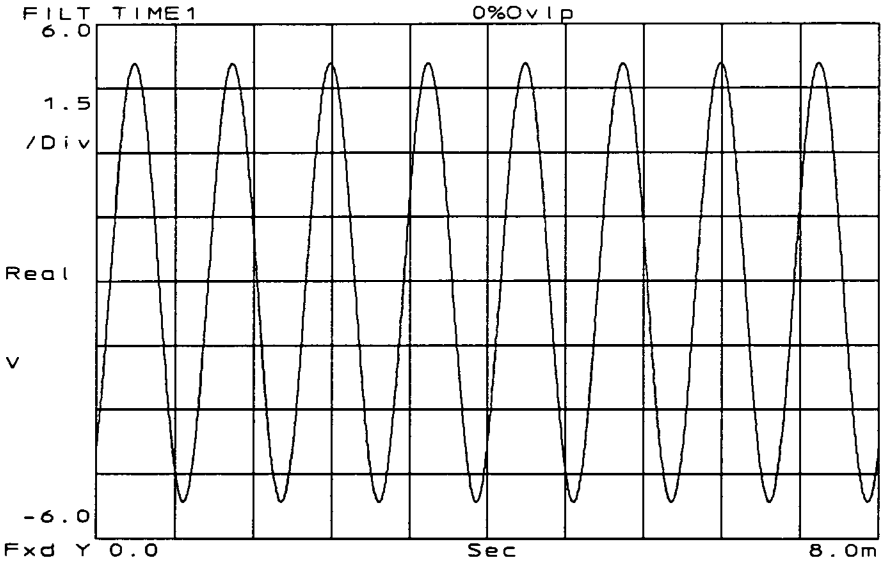


Figure 8-3. Sine Wave

If figure 8-3 is correct, the following subblocks are verified:

LO Input Receiver
Multiplier
Timing State Machine (U3)

4. Press the HP 3563A keys as follows:

[Measurement]
SOURCE ...... SOURCE TYPE ...... RANDOM NOISE

Refer to figure 8-4 to verify result.

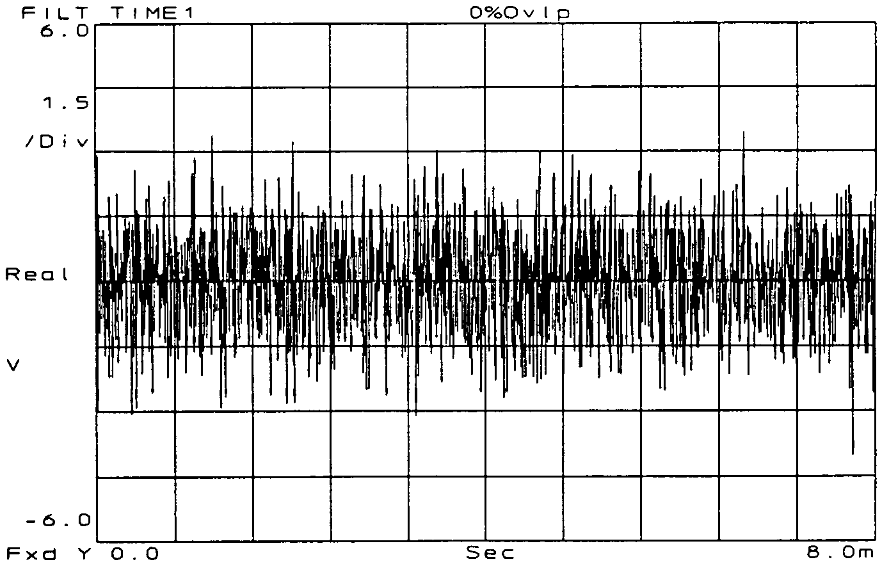


Figure 8-4. Random Noise

If figure 8-4 is correct the following subblock is verified:

Noise Generator

5. The random noise should follow the frequency span as it is changed. The display should appear similar to figure 8-4 as the frequency span is changed. To change frequency spans, press the HP 3563A keys as follows:

[Measurement]				
FREQ	......	**FREQ SPAN**	......	**1 kHz**
			......	**10 kHz**
			......	**50 kHz**

If the random noise follows the frequency span, the following subblock is verified:

Effective Sample Rate Generator

6. Press the HP 3563A keys as follows:

[Measurement]
FREQ ...... MAX
SPAN

[Display]
B

[Display]
MEAS
DISP ...... FILTRD
INPUT ...... TIME
REC 2

[Display]
SCALE ...... Y FIXD
SCALE ...... **6, −6** V

[Display]
A&B

[Measurement]
SOURCE ...... BURST
RANDOM

Refer to figure 8-5 to verify result.

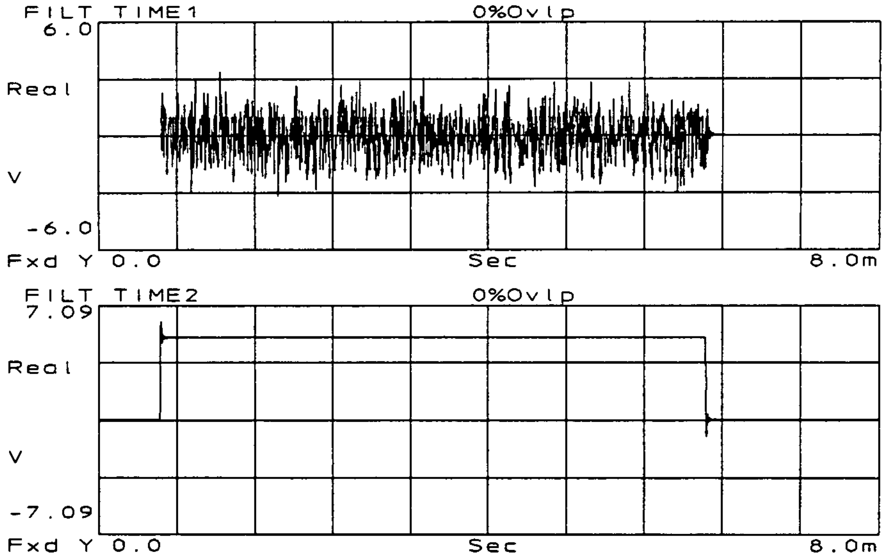


Figure 8-5. Burst Random # 1

7. Press the HP 3563A keys as follows:

⌈ Measurement ⌉
SOURCE ...... SOURCE TYPE ...... BURST RANDOM **25**
..... ENTER

Refer to figure 8-6 to verify result.

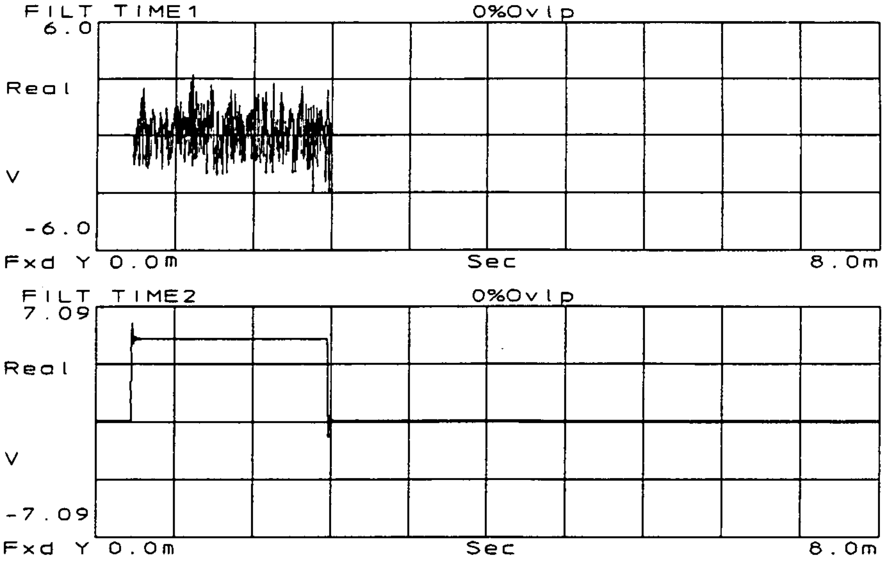


Figure 8-6. Burst Random # 2

If figures 8-5 and 8-6 are correct, the following subblock is verified:

Burst Control Circuit

8. Press the HP 3563A keys as follows:

[Measurement]
SOURCE ...... SOURCE TYPE ...... FIXED SINE ..... 1 kHz

[Input Setup]
SELECT TRIG ...... SOURCE TRIG

The source trigger point may vary on the sine wave, but the trigger point on the SYNC OUT waveform should be the same as displayed in figure 8-7.

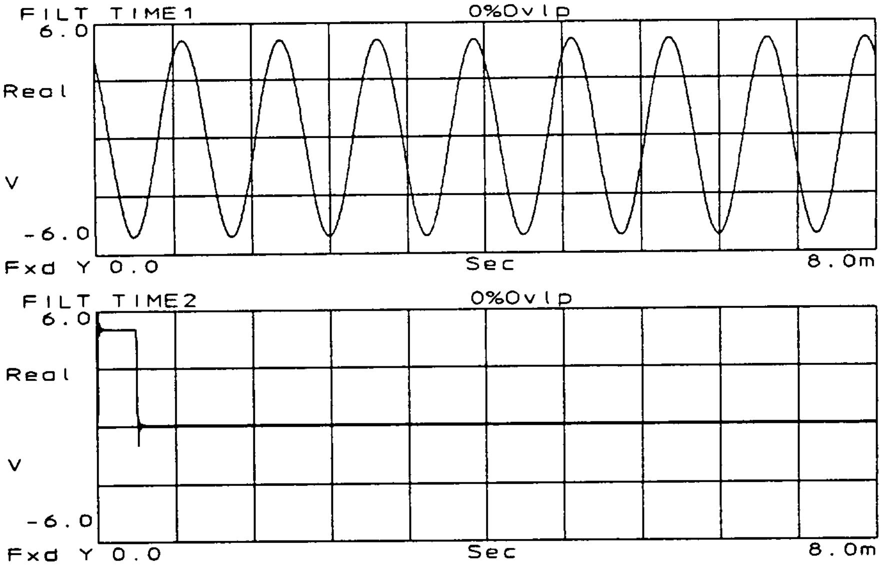


Figure 8-7. Source Trigger

If figure 8-7 is correct, the following subblock is verified:

Phase Resolution Circuit

Table 8-6. Digital Source Failures

Test Results	Most Likely Cause of Failure Troubleshoot subblocks in order listed
Digital Source Main Test Passes Digital Source Counters Passes Digital Source F/E Interface Fails Bits: 0,1,2,3,7, or 12	Control Registers (Go to "Digital Source Signature Analysis Test THREE")
Digital Source F/E Interface Passes Digital Source Counters Pass or Fail Digital Source Main Test Fails Bits: 6,9,10	Timing Control Circuit LO Input Receiver Multiplier (Go to "Digital Source Signature Analysis Tests")
Digital Source F/E Interface Passes Digital Source Counters Pass Digital Source Main Test Fails Bits: 9,10 Functions: Sine Output is defective, but Burst Random and SYNC OUT operate	LO Input Receiver (Go to "Digital Source Signature Analysis Tests")
Digital Source F/E Interface Passes Digital Source Counters Pass or Fail Digital Source Main Test Fails Bits: 9,10 Functions: Source Output Defective Random Noise Defective	Timing Control Circuit LO Input Receiver Multiplier (Go to "Digital Source Signature Analysis Tests")
Digital Source F/E Interface Passes Digital Source Counters Pass or Fail Digital Source Main Test Fails Bits: 13, 14, or 15	Phase Resolution Circuit (Go to "Digital Source Signature Analysis Tests")
Digital Source F/E Interface Passes Digital Source Counters Pass or Fail Digital Source Main Test Fails Bits: 6,9,10 and one or more of the following bits: 11,12,13,14,15	Programmable Counters Phase Resolution Circuit Timing Control Circuit (Go to "Digital Source Signature Analysis Tests")
Digital Source F/E Interface Fails Digital Source Main Test Fails Bits: Multiple Failures Functions: No functions operate	DS Data Bus System Interace Device Decoder PAL or Buffer Programmable Counters Status Registers Test Registers Control Registers' Latches (Go to "Multiple Failures Test")

Multiple Failures Test

This test verifies the DS data bus, the system interface, and the device decoder PAL and buffer.

1. Press the HP 3563A line switch OFF. Place the A1 Digital Source on the extender board.
2. Use a logic probe to verify the system interface lines are toggling between TTL level high and TTL level low. Use the following test locations:

   U404-19

   U403 pins 11, 13 through 18

3. Press the HP 3563A keys as follows:

   [Control]
   SPCL FCTN ...... SERVICE TEST ...... LOOP ON OFF
   .... TEST SOURCE ..... SOURCE MAIN

4. To verify the device decoder PAL and buffer, use a logic probe to check the following signals are the correct TTL level:

U303 pin	12 Toggling	U401 pin	2 Toggling
	13 Toggling		7 Toggling
	14 Toggling		10 Toggling
	15 Toggling		11 Toggling
	16 Toggling		
	17 High		
	18 Toggling		
	19 Toggling		

5. Press the HP 3563A keys as follows:

   RETURN ...... LOOP ON OFF
   ...... LOOP ON OFF ...... TEST SOURCE ..... FR END INTFCE

6. Use a logic probe to verify the following signals are the correct TTL level:

U303 pin	12 High
	13 Toggling
	14 High
	15 High
	16 Toggling
	17 Toggling
	18 Toggling
	19 Toggling

7. Use a logic to verify the DS data lines are togging (FR END INTFCE in loop mode). Some of the lines will toggle slowly. Use the following test locations:

   U406 pins 1 and 11 through 19

   U405 pins 11 through 18

8. Press A2 S1. After the power-up tests are complete, verify the following signals are the correct TTL level:

Test Location	Signal Name	TTL Level
U203-2	TEST	Low
U304-6	NRSTL	High
U304-9	BRST	High
U302-4	RESETL	High

9. If the fault has not been found, go to "Digital Source Signature Analysis Tests".

Effective Sample Rate Generator Test

Use table 8-7 to verify the components in the effective sample rate generator. In table 8-7, a "0" represents a TTL level low and a "1" represents a TTL level high.

Set the frequency span by pressing the HP 3563A keys as follows:

[Measurement]
FREQ ...... FREQ
SPAN ...... To frequency span in table 8-7

Table 8-7. Effective Sample Rate Generator Test

Frequency Span	DA (U1-3)	DB (U4-12)	DSEL (U101-2)	TP12
1 kHz	0	0	1	25.6 kHz
3.125 kHz	0	1	1	80.0 kHz
10 kHz	1	0	1	256 kHz
100 kHz	1	1	0	2.56 MHz

If the fault has not been found, go to the next section, "Digital Source Signature Analysis Tests".

Digital Source Signature Analysis Tests

Use these tests and the "Digital Source Waveforms" section which follows to isolate a failure on the digital source assembly. Only the components in the failing subblocks need to be tested.

Digital Source Signature Analysis Test ONE

1. Press the HP 3563A line switch OFF.
2. Connect the Signature Analyzer as follows:

Table 8-8. DS Signature Analyzer Setup

Signal	Polarity	Connection
Ground	—	A1 J2-1
Clock	Positive edge	A1 J2-3
Stop	Positive edge	A1 J2-4
Start	Positive edge	A1 J2-5

3. Press the HP 3563A line switch ON.
4. Press the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC
TEST ...... LOOP
ON OFF

...... TEST
SOURCE ..... SOURCE
MAIN

5. When finished with the test, turn the loop mode off by pressing the keys as follows:

...... RETURN ...... LOOP
ON OFF

Table 8-9. DS Signature Analysis Test ONE

Source Main Test

Source Main Test in loop mode
Jumpers in normal (N) position: All jumpers
Signature Analyzer Setup: Refer to table 8-8
+5 V Signature = H166

Component	Pin	Signature
U1	11	U233
	12	40C9
	13	C9FH
	14	7467
	15	P09H
U2	11	0765
	12	9206
	13	HA1F
	14	6P24
	15	41CF
U3	12	AU9H
	13	460C
	14	12C3
	15	49H2
	16	C26H
	17	2F90
	18	H166
	19	2FP4
U4	3	36UF
	6	H166
	8	0UH3
	11	HPC5
U5	12	H10F
	13	5791
	14	H10F
	15	9AUF
	16	6866
	17	97C4
	18	H166
	19	3486
U6	3	H10F
	6	H10F
	8	21F2
	11	H166
U7	8	0000
	9	H166
	10	5791
	12	H166
	13	H10F
U8	5	615F
	6	C03A
	8	006A
	9	H10F
U9	5	F4U5
	6	1593
	8	C88U
	9	69P9
U10	3	93AH
	4	7003
	5	01H4
	6	C93U
	10	654A
	11	0C70
	12	CF6H
	13	67P3
U11	12	5612
	13	2FU6
	14	UHAP
	15	858P
	16	5612
	17	2FU6
	18	UHAP
U12	12	127P
	13	8340
	14	7716
	15	43A6
	16	127P
	17	8340
	18	7716

DS Signature Analysis Test ONE continued

Component	Pin	Signature
U13	13	5730
U101	7	C2H9
U102	12	811H
	13	8315
	14	C957
	15	02PU
	16	5UA9
	17	PA58
	18	H166
	19	H166
U103	2	10AH
U105	4	C367
	5	H166
	7	C367
	9	0000
	14	0000
U106	5	A75U
	6	7639
	8	0000
	9	H166
U107	9	H166
	10	5791
	12	H166
	13	H10F
U108	9	H166
	10	5791
	12	H10F
	13	H10F
U109	6	H166
	8	H166
U110	3	1AUA
	4	C4A8
	5	6381
	6	8815
	10	UHHU
	11	F73A
	12	HA48
	13	54U1
U111	12	5612
	13	2FU6
	14	UHAP
	15	858P
	16	5612
	17	2FU6
	18	UHAP
	19	858P
U112	12	0PHC
	13	8340
	14	7716
	15	43A6
	16	0PHC
	17	8340
	18	7716
	19	43A6
U113	12	5UPH
U201	1	31UC
	4	F6P2
	10	304P
	13	0000
U202	6	HPC5
	10	2C66
U203	2	H166
	6	0000
	9	47HH
	12	465U
	16	UA00
U204	2	C367
	5	653U
	15	P79A
	16	0000
U209	6	7H1U
U302	4	H166
	8	H166
	10	2C66

DS Signature Analysis Test ONE continued

Component	Pin	Signature
U304	1	H166
	2	F11P
	5	7557
	6	5FF3
	8	47HH
	12	0UH3
	13	465U
	16	HPC5
	17	UA00
	19	1078
U305	2	UA00
	4	465U
	5	47HH
	9	A75U
	10	F2HP
	11	5FF3
	13	A392
	14	811H
	15	F6P2
	16	811H
	17	77P7
	18	304P

Component	Pin	Signature
U306	6	H166
U307	15	465U
	16	47HH
U308	4	UA00
	7	465U
	12	H166
U407	1	H166
	6	47HH
	7	47HH
U409	12	H166
	13	FC55
	14	H166
	15	95C3
	16	FAH9
	17	PFH9
	18	H9C3
	19	0000

Digital Source Signature Analysis Test TWO

1. Press the HP 3563A line switch OFF.
2. Set A1 J3 to test position.
3. Press the HP 3563A line switch ON.
4. Press the HP 3563A keys as follows:

[Control]
SPCL
FCTN ...... SERVIC TEST ...... LOOP ON OFF
...... TEST SOURCE ..... SOURCE MAIN

Note

DS Signature Analysis Test Two disables the feedback loop between the burst state machine (U102) and the burst control circuit's counters (U305).

Table 8-10. DS Signature Analysis Test TWO

Burst control Circuit
Source Main Test in loop mode
Jumpers in normal (N) position: All jumpers except A1 J3
Jumpers in test (T) position: A1 J3
Signature Analyzer Setup: Refer to table 8-8
+5 V Signature = H166

Component	Pin	Signature	Component	Pin	Signature
U102	12	P75H	U305	13	7U6P
	13	19C5		17	PHF6
	14	45C7			
	15	02PU			
	16	5UA9			
	17	PA58			
	18	H166			
	19	H166			

5. Put jumper A1 J3 in normal (N) position.

Digital Source Signature Analysis Test THREE

1. Set A1 J3 in normal (N) position.
2. Press A2 S1.
3. Press the HP 3563A keys as follows:

[Control]
SPCL FCTN ...... SERVIC TEST ...... LOOP ON OFF
...... TEST SOURCE ..... FR END INTFCE

Table 8-11. DS Signature Analysis Test THREE

Front End Interface Test

Front End Interface in loop mode
Jumpers in normal (N) position: All jumpers
Signature Analyzer Setup: Refer to table 8-8
+5 V Signature = 088C

Component	Pin	Signature	Component	Pin	Signature
U4	6	H359	U205	11	088C
U6	11	H359		13	FC45
U104	3	6F76	U206	7	6574
	4	HCH2		9	6HUU
	5	5289	U207	7	F472
	6	P7CC		9	FFU9
	8	0000	U208	4	95HH
	9	3U2P		5	99C5
	10	7FP2		6	U0H8
	11	6H62		7	UF01
U106	8	C49A	U302	8	CF11
U109	3	083A			
U204	1	088C			
	2	0000			
	5	8FFP			
	6	0UA9			
	9	U039			
	12	CCC3			
	15	0000			
	16	0000			
	19	0000			

Digital Source Signature Analysis Test FOUR

1. Press the HP 3563A line switch OFF.
2. Connect U311 pin 10 to TP15.
3. Press the HP 3563A line switch ON.
4. Press the HP 3563A keys as follows:

⌈ Control ⌉
SPCL FCTN ...... SERVIC TEST
- ...... LOOP <u>ON</u> OFF
- ...... TEST SOURCE ..... SOURCE MAIN

Table 8-12. DS Signature Analysis Test FOUR

Random Noise Generator Test

Source Main Test in loop mode
Jumpers in normal (N) position: All Jumpers
Connect U311-10 to TP15
Signature Analyzer Setup: Refer to table 8-8
+5 V Signature = H166

Component	Pin	Signature	Component	Pin	Signature
U208	9	C139	U313	9	7753
	10	A38A		10	HH05
	11	U732		11	5C09
	12	34P7		13	1PF9
	13	12C3		14	4F13
	14	460C		15	2F4F
U209	6	1764		16	09HF
U210	2	0000		17	2F4F
	5	2HP4	U410	1	09FA
	6	0000		2	4UH7
	9	7P38		3	4UH7
	12	F2CC		4	18AC
	15	08P1		5	18AC
	16	4H58		6	P9P2
	19	1AA4		7	P9P2
U212	1	7CC0		9	7A61
	4	6HU7		15	09FA
	10	F4PF	U411	1	09FA
	13	F322		2	4UH7
U310	2	C03A		3	4UH7
	5	8C04		4	18AC
	6	05FC		5	18AC
	9	6678		6	P9P2
	12	9508		7	P9P2
	15	2777		9	5FU5
	16	4CP8		15	09FA
	19	H0FU	U412	1	09FA
U311	2	0000		2	4UH7
	3	A431		3	4UH7
	11	H166		4	18AC
U312	1	23CH		5	18AC
	4	60FC		6	P9P2
	10	37PF		7	P9P2
	13	UA63		9	5828
				15	09FA

DS Signature Analysis Test FOUR continued

Component	Pin	Signature
U413	1	09FA
	2	4UH7
	3	4UH7
	4	18AC
	5	18AC
	6	P9P2
	7	P9P2
	9	8200
	15	09FA

Digital Source Waveforms

The oscilloscope plots are used for troubleshooting the A1 Digital Source. Note that all the measurements are taken with a **10:1** probe. Other notes unique to a measurement are written next to the waveform.

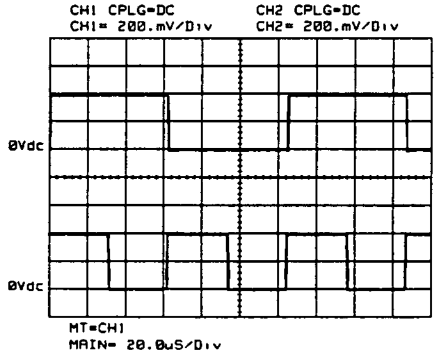
Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury.**

Table 8-13. Digital Source Waveforms

All jumpers should be in normal position
Connect ground to A1 TP1 or A1 TP15
Probe: 10:1

Press the keys as follows:

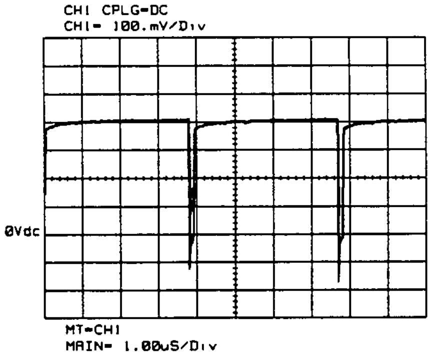
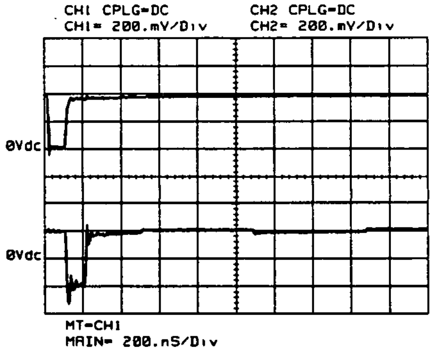
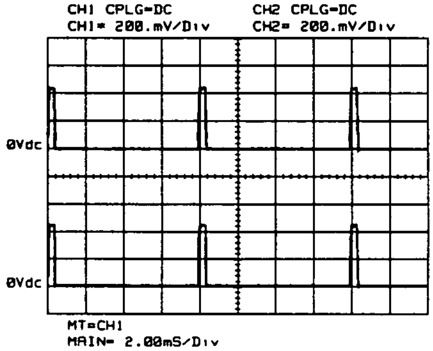
SPCL FCTN ...... SERVIC
TEST ...... LOOP
ON OFF
...... TEST
SOURCE ..... FR END
INTFCE

Setup	Parameters	Waveform
CNTLD and CNTCLK Connect CH1 to A1 TP10 Connect CH2 to A1 TP11 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 20 μs/Div Trigger CH1	Time Relationship	 **#1**

After viewing waveform, press A2 S1.

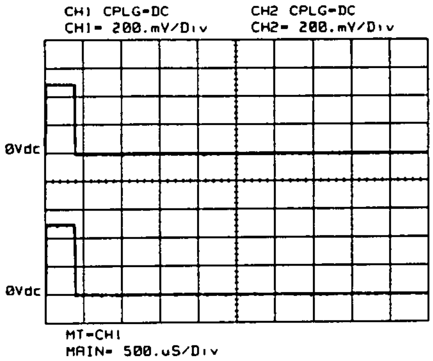
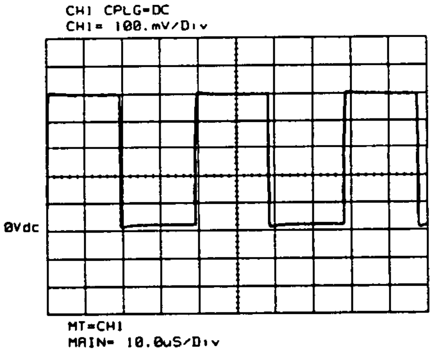
Digital Source Waveforms continued

All jumpers should be in normal position
Connect ground to A1 TP1 or A1 TP15
Probe: 10:1

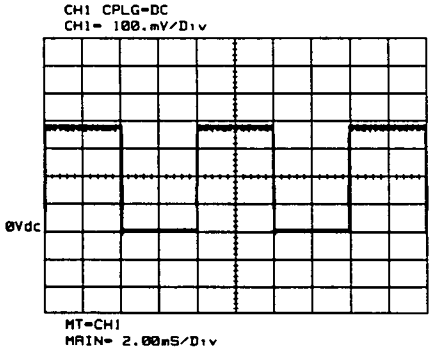
Setup	Parameters	Waveform
LOL Connect CH1 to A1 TP2 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 μs/Div Trigger CH1	Time	 #2
LOL and CLRL Connect CH1 to A1 TP2 Connect CH2 to A1 TP3 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 200 ns/Div Trigger CH1	Time Relationship Duty Cycle	 #3
NCLK and NSYNC Connect CH1 to A1 J701-3 Connect CH2 to A1 U11-2 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 ms/Div Trigger CH1	Time Relationship	 #4

Digital Source Waveforms continued

All jumpers should be in normal position
Connect ground to A1 TP1 or A1 TP15
Probe: 10:1

Setup	Parameters	Waveform
BSNC and SYNC OUT Connect CH1 to A1 U103-12 Connect CH2 to A1 U301-1 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 500 μs/Div Trigger CH1	Time Relationship	 #5
Press the keys as follows: **FREQ** ...... FREQ SPAN ...... 1 kHz		
10× Effective Sample Rate Connect CH1 to A1 TP12 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 10 μs/Div Trigger CH1	Time Duty Cycle	 #6
After viewing waveform, press MAX SPAN.		

Digital Source Waveforms continued

<table>
<tr><td colspan="3">All jumpers should be in normal position
Connect ground to A1 TP1 or A1 TP15
Probe: 10:1</td></tr>
<tr><th>Setup</th><th>Parameters</th><th>Waveform</th></tr>
<tr><td colspan="3">Connect the front panel source output to external trigger and Channel 1.
Press the keys as follows:
<b>SOURCE</b> ...... SOURCE LEVEL ...... 5 V
...... SOURCE TYPE ...... FIXED SINE ......125 Hz
<b>SELECT TRIG</b> ..... MORE TYPES ...... EXT TRIG</td></tr>
<tr><td><b>TRIG</b>
Connect CH1 to A1 U5-7
Oscilloscope:
CH1 V/Div 100 mV/Div
CH1 Coupling dc
Time/Div 2 ms/Div
Trigger CH1</td><td>Time
Duty Cycle</td><td>
#7</td></tr>
</table>

Digital Source After-Repair Adjustments and Tests

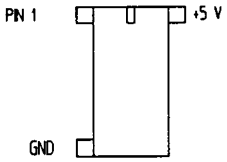
Table 8-14. After-Repair Adjustments and Tests

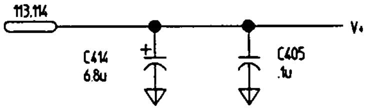
Perform the following:*	Section
Diagnostic Tests: FR END INTFCE SOURCE MAIN TEST ALL	VII
Adjustments: None	III
Performance Tests: If the noise generator subblock was repaired; perform the Source Energy Measurement test.	II (Chapter 4, *HP 3563A Installation Guide*)
Operational Verification: If the phase resolution circuit was repaired; perform the Signal Channel Phase Accuracy test. If the LO Input Receiver was repaired; perform the Source Amplitude Accuracy and Flatness test.	II (Chapter 3, *HP 3563A Installation Guide*)

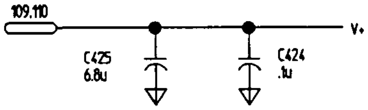
*Return all jumpers to the normal (N) position.

IC	GND	+5V	V+	V-
U1	8			
U3	11			
U5	11			
U7				
U8	7			
U9	7			
U13	6,8			
U14		10,14		
U101	1			
U102	11			
U105	1,10,11			
	12,13,15			
U113	1,3,10			
	17,18,19			
U205	1,5,8			
	9,10,15			
U206	8,10,15			
U207	8,10,15			
U208	8,15			
U209	8,9,10			
U212	7,8			
U301	2,11			
U308	15			
U313	12,18 19,20	21,24		
U404	1,3,5,7			
	9,10,17, 18			
U407	15			
U409	1			
U414			7	4
U415			8	4

ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED TO PIN 8 AND +5 V IS CONNECTED TO PIN 16).



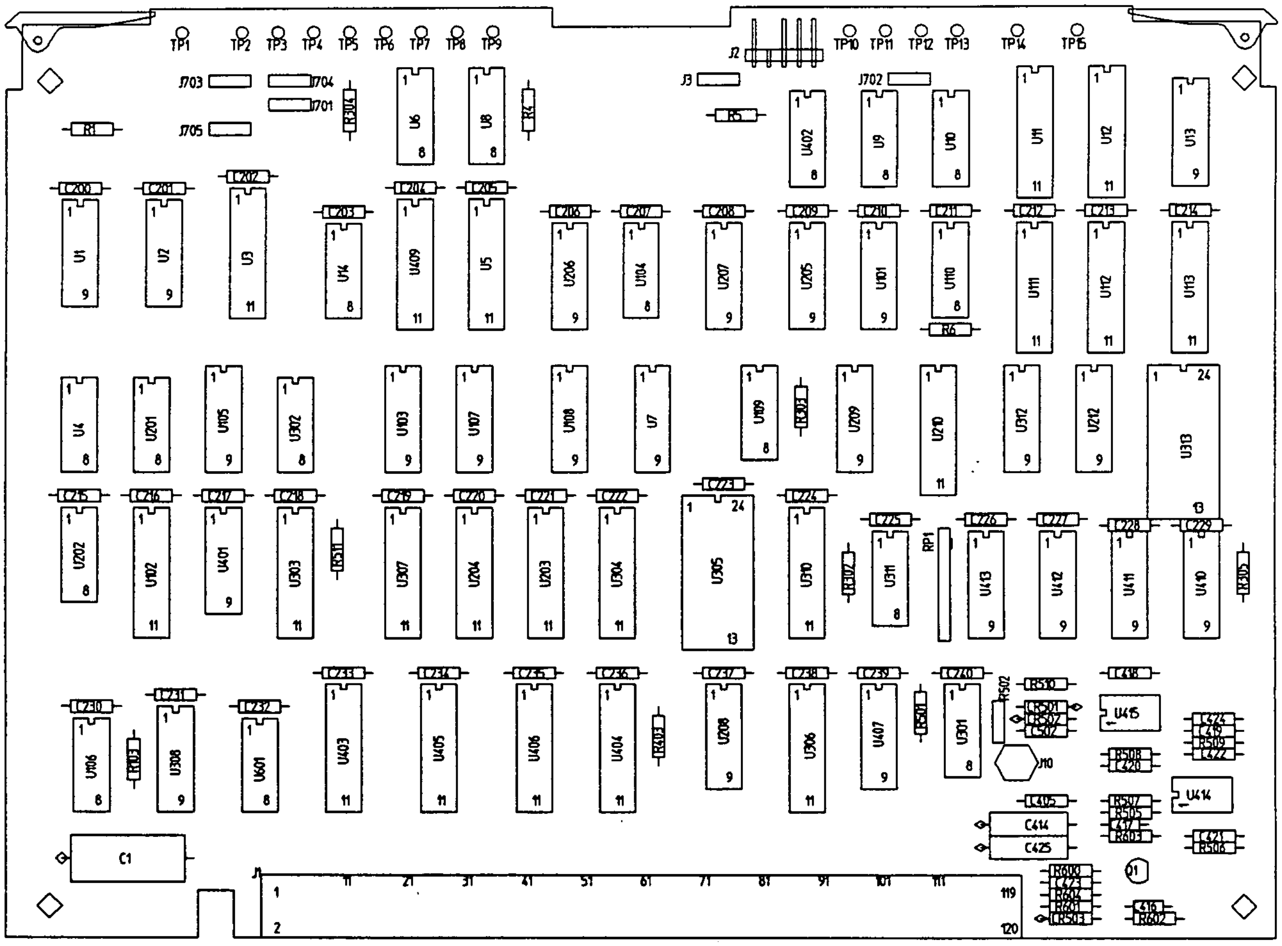




A1 Digital Source Ground and Power Chart

P/N 03562-66501 Rev B

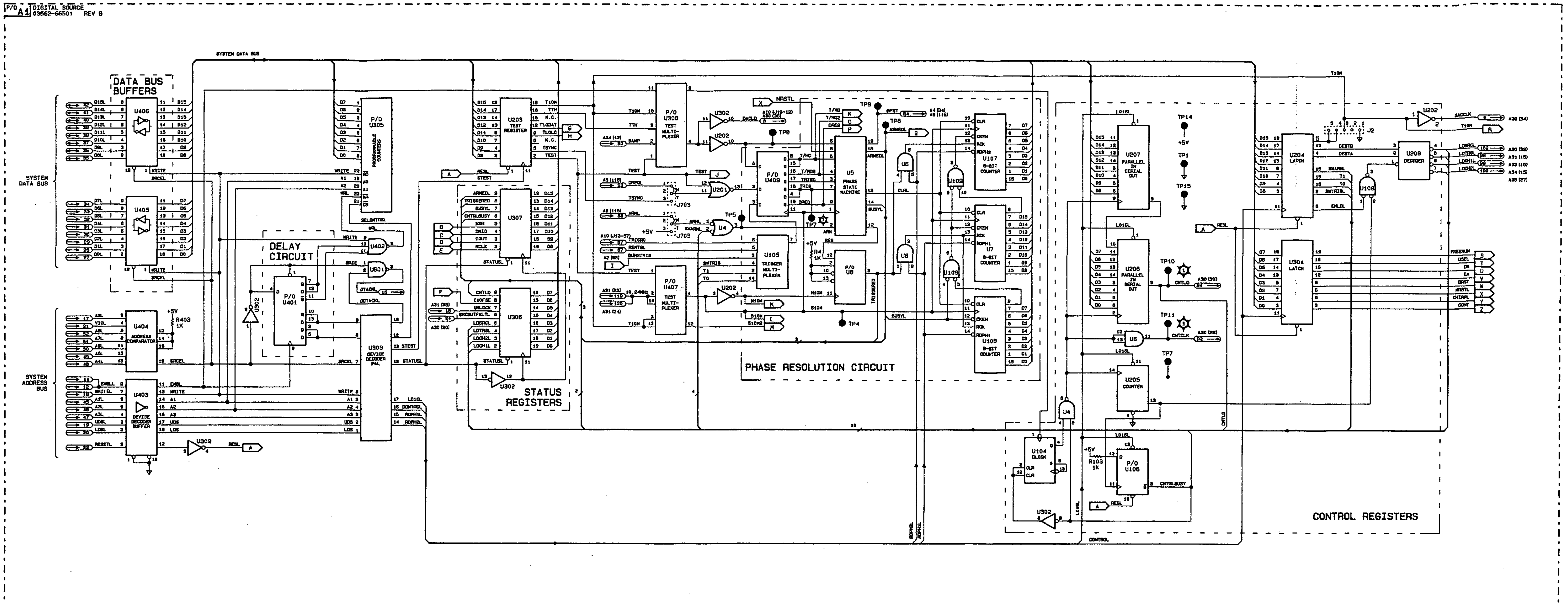
COMPONENT LOCATOR REV B



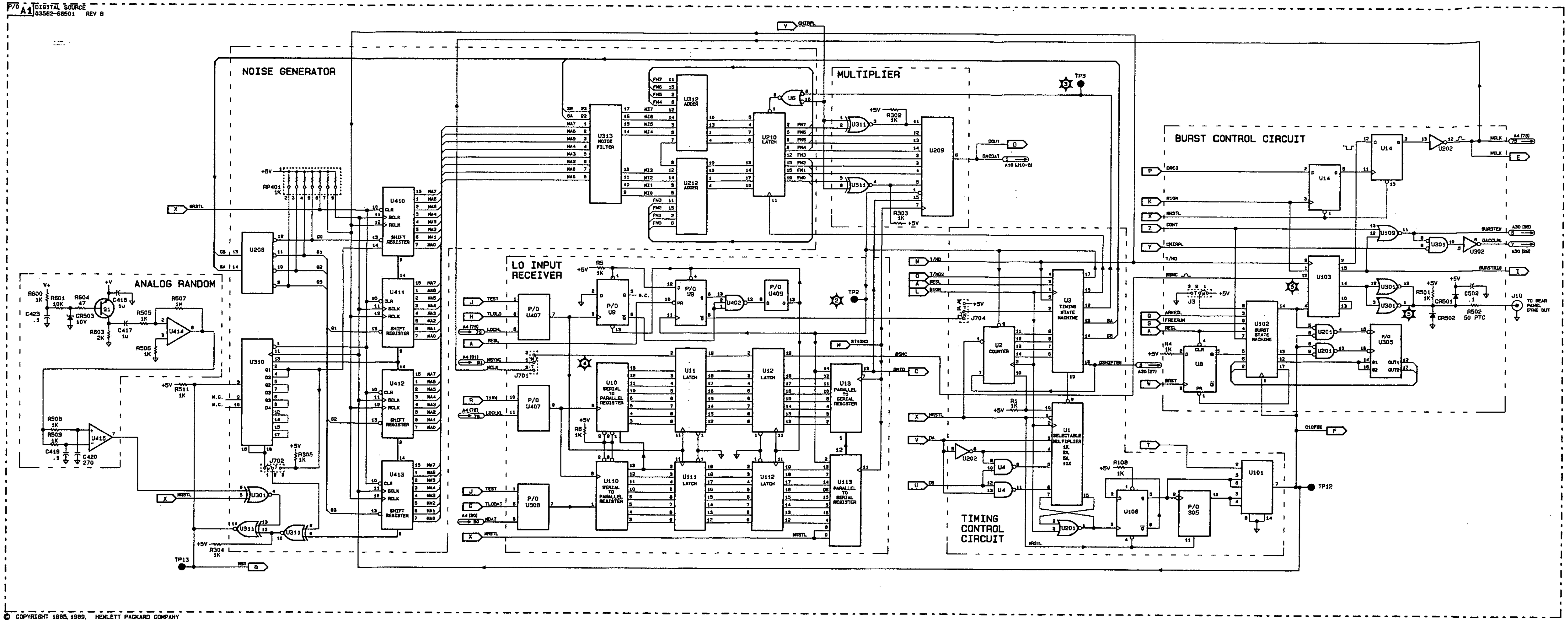
A1 Digital Source Component Locator

P/N 03562-66501 Rev B

Page 2 of 4



A1 Digital Source Schematic
P/N 03562-66501
Page 3 of 4



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A1 Digital Source Schematic
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A2, A22
System CPU/HP-IB

A2, A22 System CPU/HP-IB

The information in this section should be used to isolate faulty subblocks in the A2 and A22 System CPU/HP-IB assemblies. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the Circuit Descriptions of Section VI are understood.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

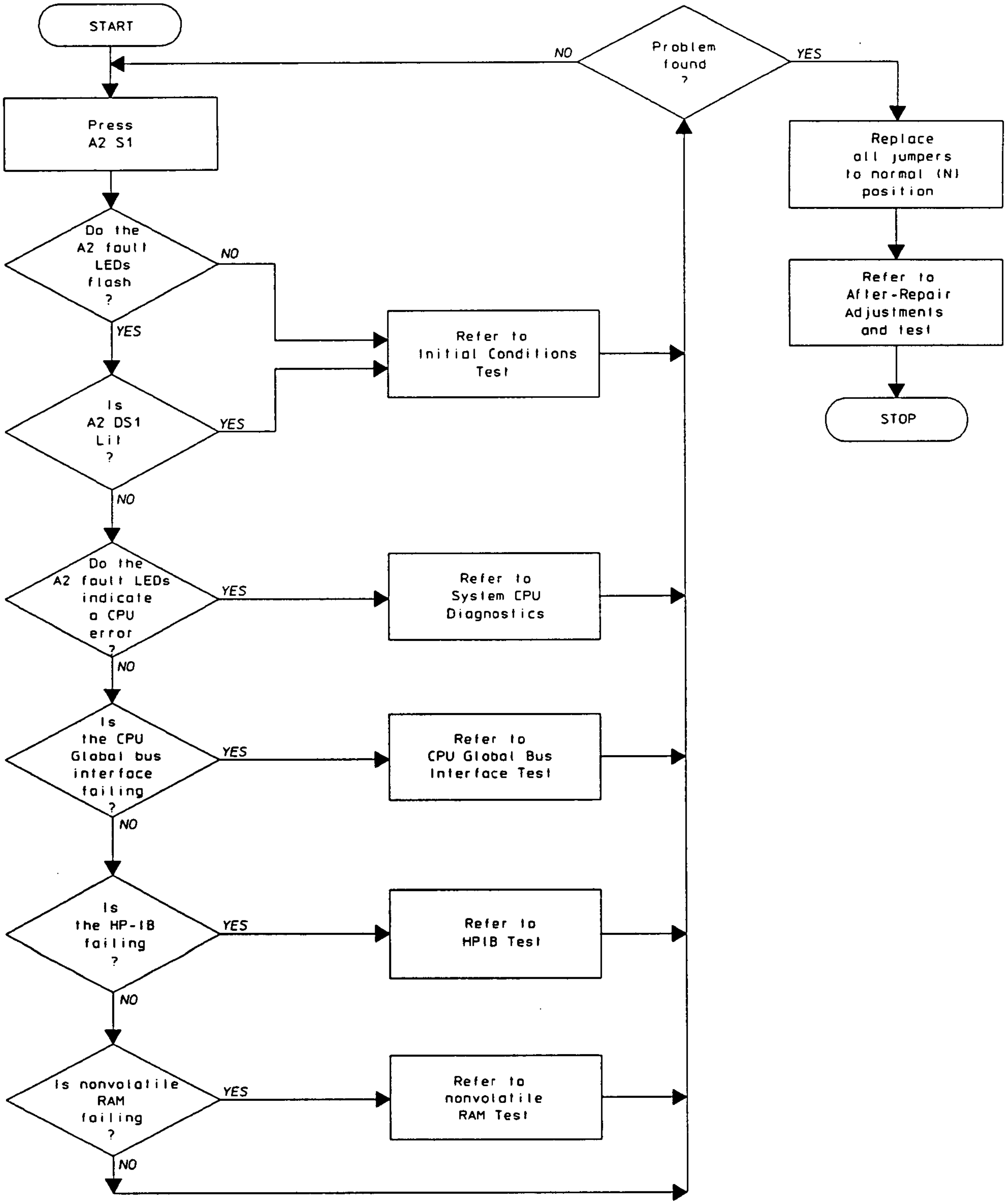
Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	Start troubleshooting by using figure 8-8. This procedure diagram describes the best order to perform the troubleshooting tests based on the symptoms observed.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
Verify	Use the oscilloscope waveforms in table 8-19 to see correct operation at various test points in the assembly.
After-Repair	Use table 8-20 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. Only +5 Vdc and ground are required to troubleshoot the A2 CPU/HP-IB assembly. To run the A2 CPU/HP-IB assembly without the rest of the instrument, put jumpers A2 J15 and A2 J16 in test (T) position.
2. The A2 CPU/HP-IB can be run on an external clock by grounding A2 TP3 and connecting a TTL level, 8 MHz clock to A2 TP4.
3. Undefined failures are most likely caused by stuck bits. This is occurring if the status LEDs (A2 DS2) are a steady state value instead of changing rapidly. Go to the "CPU/HP-IB Initial Conditions Test."



START
Press A2 S1
Do the A2 fault LEDs flash ?
NO
YES
Is A2 DS1 Lit ?
YES
NO
Refer to Initial Conditions Test
Do the A2 fault LEDs indicate a CPU error ?
YES
NO
Refer to System CPU Diagnostics
Is the CPU Global bus interface failing ?
YES
NO
Refer to CPU Global Bus Interface Test
Is the HP-IB failing ?
YES
NO
Refer to HPIB Test
Is nonvolatile RAM failing ?
YES
NO
Refer to nonvolatile RAM Test
Problem found ?
NO
YES
Replace all jumpers to normal (N) position
Refer to After-Repair Adjustments and test
STOP

Figure 8-8. System CPU/HP-IB Troubleshooting Procedure Diagram

CPU/HP-IB Initial Conditions Test

1. Disconnect the power cable from the rear panel and remove the top cover. Place the A2 CPU/HP-IB on the extender board.

2. Connect the power cable and press the HP 3563A line switch ON.

3. Check the following for correct value:

Signal	Location	Value
+5S	A2 TP2	+5 +0. 3V
PWRUP	A2 J15-2	TTL logic 1
PWRDNL	A2 J16-2	TTL logic 1
HALTL	A2 U100-17	TTL logic 1
RESETL	A2 U100-18	TTL logic 1
8 mHz Clock	A2 TP5	Refer to Waveform #1 (CPU Signal Waveforms)

4. If the +5S PWRUP, or PWRDNL are not the correct values, go to the "A18 Power Supply Assembly" troubleshooting procedures.

5. If the cause of the failure is still not found, go to the "CPU Signature Analysis Tests."

System CPU Diagnostics

The CPU diagnostics do the following at turn on or when the CPU is reset by pressing A2 S1:

1. Flashes the LEDs and then turns each one on starting with DS3-1 (MSB).
2. Clears the test log.
3. Stores address and contents of NVRAM.
4. Check sums the monitor ROM.
5. Exercises several system processor (U100) instructions.
6. Tests the monitor RAM by writing and reading patterns to and from it.
7. If an error was found in the RAM test, the address decoder is exercised by writing addresses to several locations and reading the contents.
8. Tests the NVRAM using a write/read/restore sequence on each memory location.
9. Tests the timer and interrupt circuits.

The CPU diagnostics stop when a fault is found and display the error code on the test LEDs (A2 DS3, A2 DS4). If no error is found on the A2 CPU/HP-IB assembly, the power-up sequence continues. Use table 8-15 to determine the most likely failure causing an A2 CPU/HP-IB error code.

Table 8-15. System CPU/HP-IB Diagnostics

Hex Error Code	Test Description	Hex Code Explaination	Most likely Failure
Undefined	Initial Turn On	Low level fault	CPU/HP-IB Initial Conditions Test
01	Monitor Rom Check sum	Upper byte failure Lower byte passes	A2 U105
02	Monitor Rom Check sum	Lower byte failure Upper byte passes	A2 U205
03	Monitor Rom Check sum	Both bytes fail	Go to SA (F)
04	Monitor Rom Check sum	Both bytes pass	Go to SA (F)
05	Instruction Test	U100 test passes	Go to SA (F)
06	Instruction Test	U100 test fails	A2 U100
10	Monitor RAM Test	High byte, MEM0L fails	A2 U110
11	Monitor RAM Test	Low byte, MEM0L fails	A2 U210
12	Monitor RAM Test	Both MEM0L bytes fail	A2 U110, U210
13	Monitor RAM Test	High byte MEM1L	A2 U109
14	Monitor RAM Test	Low byte MEM1L	A2 U209
15	Monitor RAM Test	Both MEM1L bytes fail	A2 U109, U209
16	Monitor RAM Test	High byte MEM2L fails	A2 U107
17	Monitor RAM Test	Low byte MEM2L fails	A2 U207
18	Monitor RAM Test	Both MEM2L bytes fail	A2 U107, U207
19	Monitor RAM Test	Multiple Monitor RAM failures	Go to SA (F)
1A	Monitor RAM Test	NVRAM,bytes high fails	A2 U212
1B	Monitor RAM Test	NVRAM,bytes low fails	A2 U211
1C	Monitor RAM Test	Both NVRAM bytes fail	A2 U212 U211
C"N"	Monitor RAM Test	RAM address test fails	Line A"N"
0C	Timer and Interrupt Test	Unexpected timer interrupt	A2 U500, U413
0D	Timer and Interrupt Test	Timer interrupt failure	A2 U500, U413, A2 U100
0E	Timer and Interrupt Test	Timer Failure	A2 U413
0F	HP-IB Test	HP-IB Failure	HP-IB subblock

CPU Global Bus Interface Test

1. Press the HP 3563A line switch OFF.
2. Remove the following assemblies:

   A5 Digital Filter
   A7 Floating Point Processor
   A9 Fast Fourier Processor

3. Press the HP 3563A line switch ON.
4. Put A2J8, A2J12, A2J13, and A2J17 in test (T) position.
5. Repeatedly press the reset switch S1 while checking for TTL levels of the global bus drivers, latches, and control subblocks.

HP-IB Test

1. To test the HP-IB subblock press the HP 3563A keys as follows:

```
[ Control ]
  SPCL
  FCTN     ......   SERVIC
                    TEST      ......   TEST
                                       PROC

                              ......   TEST
                                       CPU      .....   HP-IB
                                                        DIAG
```

2. If this test passes, all signal paths and the pass through registers (A2 U112, A2 U113) are all right.
3. To check the HP-IB connector press the following keys:

```
[ Control ]
  SPCL
  FCTN     ......   SERVIC
                    TEST      ......   LOOP
                                        ON OFF

                              ......   TEST
                                       PROC

                              ......   TEST
                                       CPU      .....   HP-IB
                                                        CONNEC
```

4. Using a small jumper, short each of the control pins to the HP-IB connector ground. When a pin is grounded, the corresponding pin shown in the display should have a dot in it.
5. If this test passes, the HP-IB connector is functioning properly.

Note Remove the fan (MP209) before attempting to remove the A22 HP-IB board.

Nonvolatile RAM Test

1. Check the following for correct value:

Location	Value
U211-28	≥ 4.5V
U212-28	≥ 4.5V
U211-26	Clocking Signal
U212-26	Clocking Signal

2. Press the HP 3563A line switch off. With the power off, U211-28 should be greater than 3V.
3. Connect the signature analyzer according to table 8-16.
4. Check the signatures of A2 U408-6 and A2 U305-15, they should be the same.

CPU Signature Analysis Tests

These tests are used when the previous tests fail to find the problem.

1. Disconnect the HP 3563A power cable.
2. Put the following jumpers in test (T) position:

   A2J4, A2J5, A2J6, A2J7, A2J9, A2J10, A2J18

3. Put A2 J11 and A2 J14 in position "2".
4. Connect the signature analyzer according to table 8-16.

Table 8-16. CPU Signature Analyzer Setup

Signal	Polarity	Connection
Ground	—	A2 J2-1
Clock	Positive edge	A2 J2-3
Stop	Negative edge	A2 J2-4
Start	Negative edge	A2 J2-5

5. Connect the power cable and press the HP 3563A line switch ON.

Table 8-17. CPU Signature Analysis Test ONE

Address Test

Jumpers in test (T) position: A2J4,A2J5,A2J6,A217,A2J9,A2J10
Jumpers in position "2": A2J11,A2J14,
Jumpers in normal (N) position: A2J1,A2J8,A2J17,A2J12,A2J13,
Jumpers in either normal or test position: A2J15 A2J16,
Signature Analyzer Setup: Refer to table 8-16,
+5 V Signature = 0001

Component	Pin	Signature	Component	Pin	Signature
U100	29	UUUU	U100	37	HC89
	30	5555		38	2H70
	31	CCCC		39	HPP0
	32	7F7F		40	1293
	33	5H21		41	HAP7
	34	0AFA		42	3C96
	35	UPFH		43	3827
	36	52F8		44	755U

Put jumper J1 in position "1". Press A2 S1 (reset switch). It takes about 20s for each of the following signatures to stabilize.

+5 V Signature = 6PCP (TP2)

Component	Pin	Signature	Component	Pin	Signature
U100	45	2595	U305	14	0000
	46	1F8F		15	21P1
	47	U97F		16	1582
	48	5A34		17	AC4F
	49	6PCP		18	012U
	50	91FC	U606	13	443U
	51	3CPF		15	6PCP
	52	A70F		16	AP18
U305	10	4CAH		17	A52A
	11	U001		18	UA2U
	12	122P			
	13	6PCP			

6. If the signatures in table 8-17 are incorrect, check that A2 U100 pins 12, 13, 21, 22, 23, 24, and 25 are a TTL logic high.

7. Put A2 J1 in position “2”. It takes about 10s for each of the signatures in table 8-18 to stabilize.

Table 8-18. CPU Signature Analysis Test TWO

Monitor ROM Test

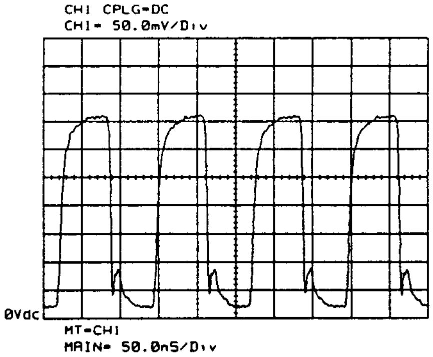
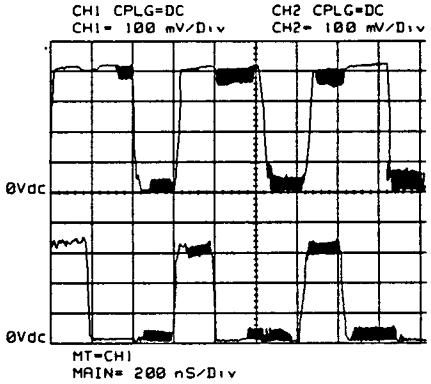
Jumpers in test (T) position: A2J4,A2J5,A2J6,A2J7,A2J9,A2J10
Jumpers in position “2”: A2J1,A2J11,A2J14
Jumpers in normal (N) position: A2J8,A2J17,A2J12,A2J13
Jumpers in either normal or test position: A2J15,A2J16
Signature Analyzer Setup: Refer to table 8-16
+5 V Signature = 6PCP

Component	Pin	Signature	Component	Pin	Signature
U105	11	57U1	U205	11	0HA4
	12	1C5F		12	5598
	13	UPCA		13	764P
	15	U818		15	HPC9
	16	5P50		16	1768
	17	2478		17	80A0
	18	6575		18	1H26
	19	AH97		19	P4FF

CPU Signal Waveforms

The oscilloscope plots are used for troubleshooting the A2 CPU/HP-IB. Note that all the measurements are taken with a **10:1** probe. Other notes unique to a measurement are written next to the waveform.

Table 8-19. CPU Signal Waveforms

Remove Power Jumpers in normal (N) position: All jumpers Connect ground to A2 TP1 Probe: 10:1 Power On		
Setup	**Parameters**	**Waveform**
8 MHz Clock Connect CH1 to A2 TP5 Oscilloscope: Bandwidth Limit: ON Mode A CH1 V/Div 50 mV/Div CH1 Coupling dc Time/Div 50 ns/Div Trigger CH1	Time Pulse shape	 **#1**
Press A2 S1 switch to see the waveform #2. DTACKL and ASL will stop changing for a short time (2s)		
DTACKL, ASL Connect CH1 to A2 U100-10 Connect CH2 to A2 U100-6 Oscilloscope: Bandwidth Limit: ON Mode A&B CH1 V/Div 100 mV/Div CH2 V/Div 100 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 200 ns/Div Trigger CH1	Time relationship	 **#2**

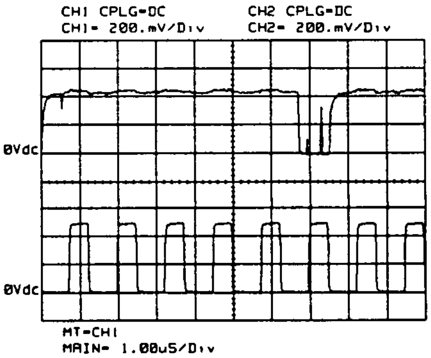
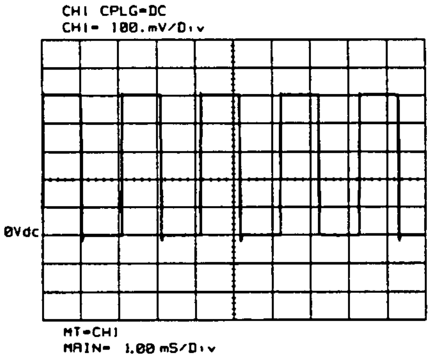
CPU Signal Waveforms continued

Remove Power
Jumpers in normal (N) position: All jumpers
Connect ground to A2 TP1
Probe: 10:1
Power On

To display waveform #3 , press the HP 3563A keys as follows:

SPCL
FCTN ...... SERVIC
TEST ...... LOOP
ON OFF

TEST
SOURCE ..... LO DSA
PATT1

Setup	Parameters	Waveform
VMAL, ENBL Connect CH1 to A2 U100-19 Connect CH2 to A2 U100-20 Oscilloscope: Bandwidth Limit: ON Mode A&B CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1.0 μs/Div Trigger CH1	Time Pulse shape	 **#3**
Press RETURN .... LOOP ON OFF		
ERROUT Connect A2 TP6 to A2 TP1 Connect CH1 to A2 U404-7 Oscilloscope: Mode A CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 ms/Div Trigger CH1	Time	 **#4**

CPU/HP-IB After-Repair Adjustments and Tests

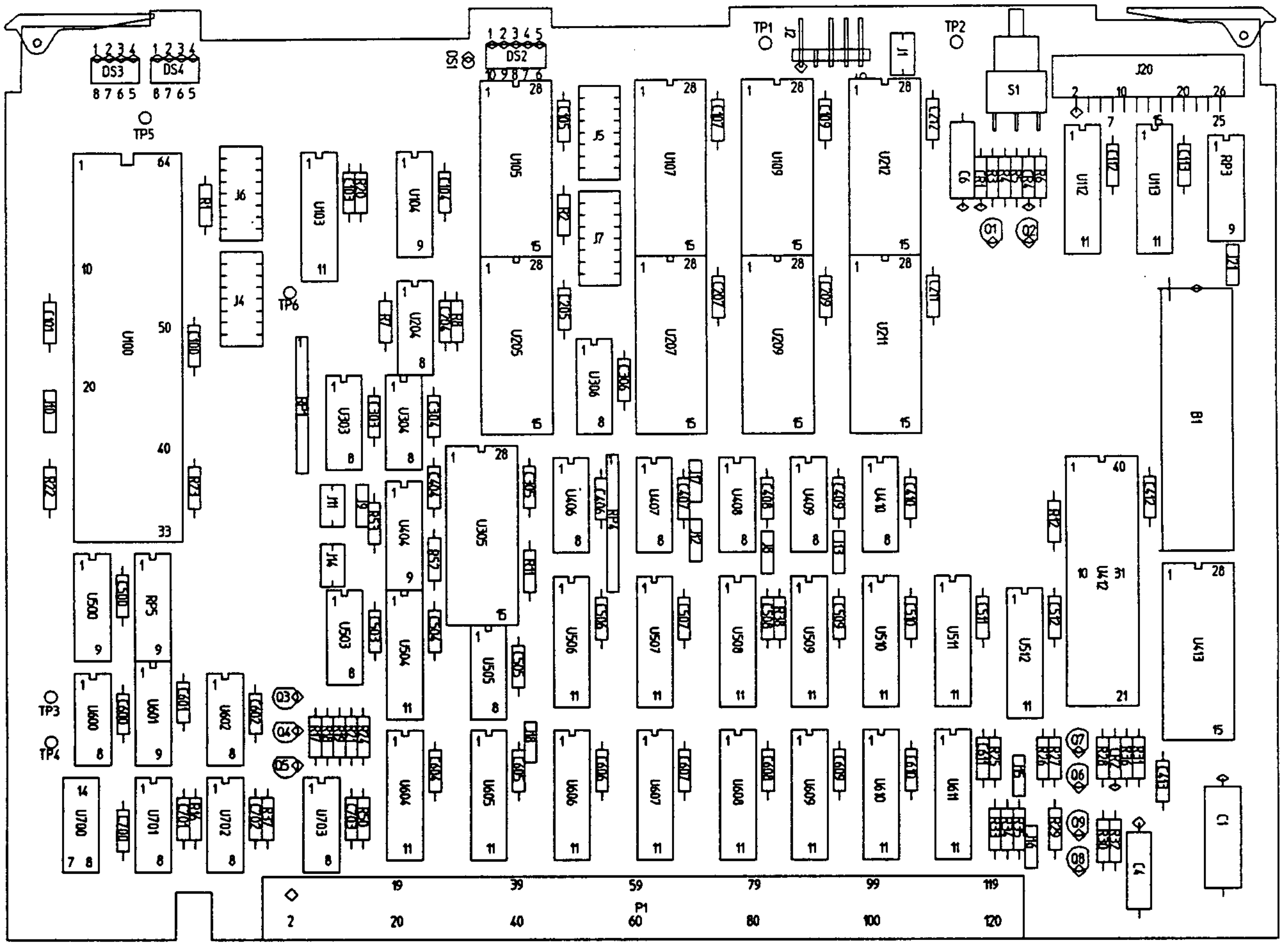
Table 8-20. After-Repair Adjustments and Tests

Perform the following:*	Section
Diagnostic Tests: TEST ALL	VII
Adjustments: None	—
Performance Tests: None	—

*Return all jumpers to the normal (N) position

IC	GND	+5V	CAPS	BAT-TERY	NO CONNECTION
U100	16,53	14,49	C1000 C100		
U103	10	20	C104		
U104	8	16	C103		11,12,15
U105	14	1,28	C105		
U107	14	28	C107		1
U109	14	28	C109		1
U110	14	28	C110		1
U112	10	20	C112		
U113	10	20	C113		
U204	7	14	C204		
U205	14	1,28	C205		
U207	14	28	C207		1
U209	14	28	C209		1
U210	14	28	C210		1
U211	14		C211	28	1
U212	14		C212	28	1
U303	7	14	C203		
U304	7	14	C304		
U305	14	28	C305		1
U306	7	14	C307		
U404	8	16	C404		3,6,9,12,13
U406	7	14	C406		
U407	7	14	C309		5,8
U408	1,7		C406	14	
U409	7	4,10 13,14	C408		5,6,8,9,11,12
U410	7	14	C409		5,6,10,11,12,13
U412	20	40	C412		1
U413	1	14	C413		3,6,27
U500	8	16	C500		14,15
U503	3,4,7 11,13	14	C503		3,4,5,6,10,11,12,13
U504	10	20	C504		1,7,8,15,17,18,19
U505	7	14	C505		3,10,11,12,13
U506	10	20	C606		
U507	10	20	C605		
U508	10	20	C508		1,6,8,9,11,12,14,19
U509	10	20	C509		
U510	10	20	C510		
U511	10	20	C511		
U512	10	20	C512		
U600	7, 9, 13	14	C600		
U601	8	16	C601		8,10,11,12
U602	3,5,7 9, 11, 13	14	C502		3,4,5,6
U604	10	20	C604		4,6,8,10,12
U605	10	20	C506		
U606	10	20	C507		14
U607	10	20	C607		
U608	10	20	C608		
U609	10	20	C609		3,11
U610	10	20	C610		
U611	10	20	C611		
U700	7	14	C700		1,2,3,4,5,6,9 10,11,12,13
U701	7	14	C701		
U702	7	14	C702		3,11
U703	7	14	C703		3,11

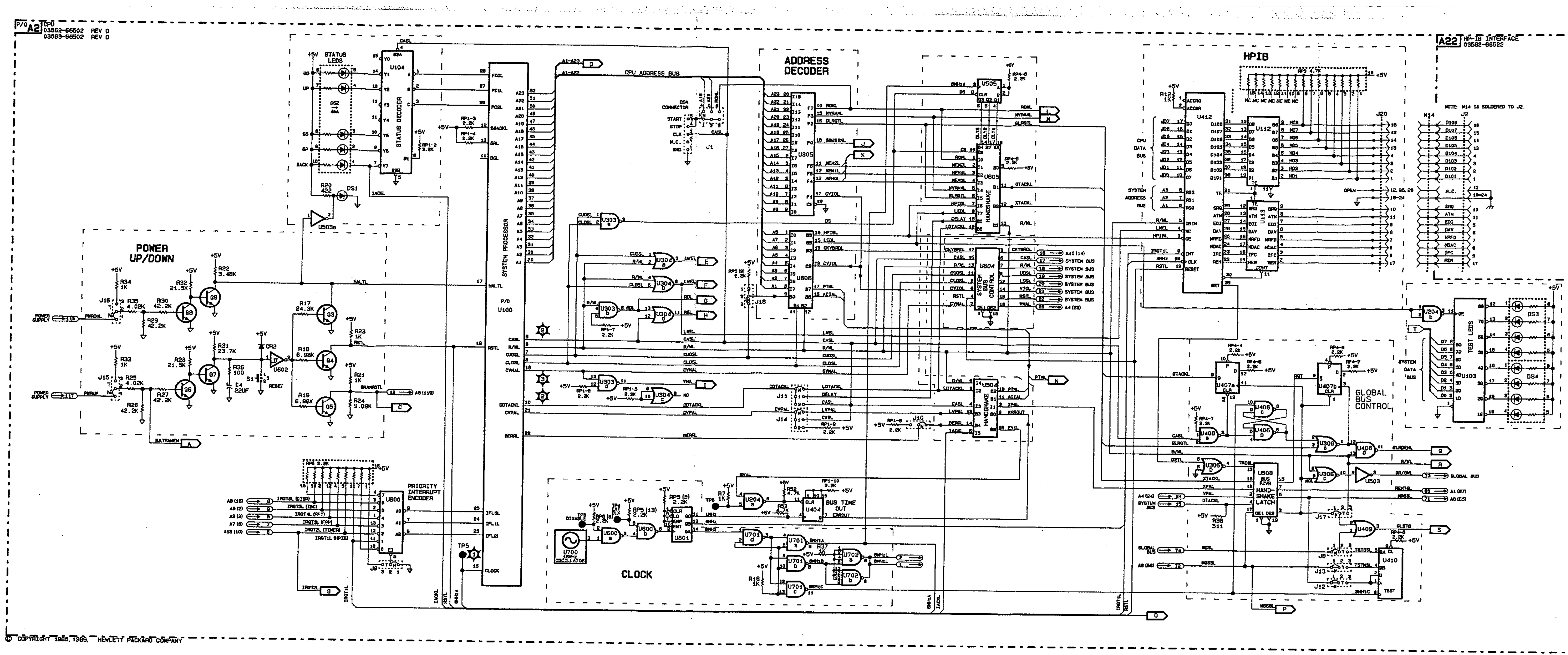
A2 Ground & Power Chart
P/N 03563-66502 Rev C



A2, A22 System CPU / HP-IB Component Locator

P/N 03563-66502 Rev D

P/N 03562-66522 Rev D



A2, A22 System CPU / HP-IB Schematic
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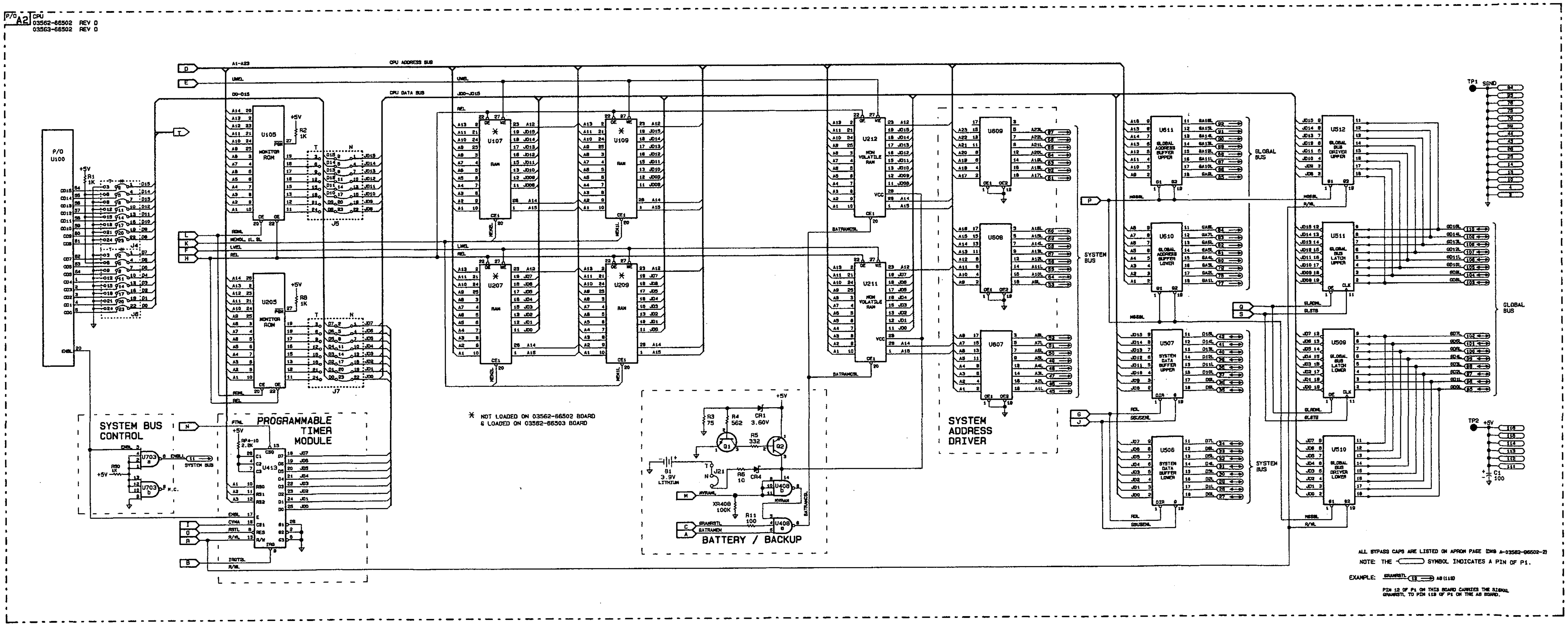

ALL BYPASS CAPS ARE LISTED ON APRON PAGE (DWG A-03562-66502-2)

NOTE: THE ⊂⊃ SYMBOL INDICATES A PIN OF P1.

EXAMPLE: GRANRSTL (12 → A8 (119)

PIN 12 OF P1 ON THIS BOARD CARRIES THE SIGNAL GRANRSTL TO PIN 119 OF P1 ON THE A8 BOARD.

A2, A22 System CPU / HP-IB Schematic
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A9 Fast Fourier Transform
(FFT) Processor

A9 Fast Fourier Transform (FFT) Processor

The information in this section should be used to isolate faulty subblocks on the FFT board. All procedures assume that you have used the fault isolation procedures in Section VII to determine that this board has failed and that you have read and understand the circuit descriptions in Section VI.

Warning

Service procedures described in this section are performed with protective covers removed and power applied. Hazardous voltages in these circuits can cause personal injury if contacted. Servicing must be preformed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A while power is on. Power transients caused by insertion or removal may cause damage to circuits on the board being changed or on other boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	To troubleshoot the FFT board, use the FFT diagnostic tests to further isolate the problem. Circuit descriptions in Section VI provide the background for understanding how the FFT board circuits work.
Procedure	Once the problem has been localized to a block of circuits, one of the three digital signature analysis (SA) tests should be used to troubleshoot individual circuits. Waveforms are provided in table 8-27 to demonstrate the correct appearance of the SA clock and start/stop signals.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. Refer to figure 4-1 in Section IV for the location of cables and boards.
After-Repair	Use table 8-28 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. The FFT status LEDs should be OFF during normal operation. They are not used to service the board.
2. A major portion of the FFT process is addressing. Be sure you understand which parts of the circuit are part of the addressing block. Refer to the block diagrams in the circuit descriptions in Section VI.

FFT Diagnostics

The diagnostic tests for the FFT board allow you to test groups of circuits to further isolate a problem. A subset of the FFT diagnostic tests run when the instrument power is turned ON, during SELF TEST, or during TEST ALL. Display the FFT-diagnostic test menu using the following sequence of keystrokes:

[Control]
PRESET ...... RESET

[Control]
SPCL
FCTN ...... SERVIC TEST ...... TEST PROC

...... TEST FFT

The menu now contains the following entries of FFT diagnostics tests:

FFT FUNCTN
FFT STATUS
FFT INTRPT
FFT RAM
FFT ROM
FFT GL INTFC

Details of each test follows.

FFT Function Test This test performs all the tests found in the rest of the menu (status, interrupt, RAM, ROM, and global interface tests). It also exercises the FFT functions by performing a forward and a reverse FFT, and Hanning, uniform, flattop, and user-defined windows on a known block of data. The resulting checksum is compared to a known value by the CPU.

If the FFT function test fails but the analyzer appears to work correctly when analyzing a fixed sine signal and all the rest of the diagnostic tests for this board pass, investigate the pseudorandom number generation block. It is reset prior to doing the math for the special functions of this test so that the resultant checksum is repeatable. If the PRN generator is not reset or does not operate correctly, the checksum generated won't always agree with the stored checksum.

The FFT function test is the most extensive diagnostic test available to test the FFT board. It is executed as a subset of the tests performed whenever the SELF TEST and TEST ALL tests are run.

FFT Status Test This test quickly checks the operation of the system bus operation between the CPU and the FFT boards. The CPU addresses the FFT board and loads a command to it which causes the FFT microprocessor to return the CPU command data. This tests the system interface circuits (in both directions), the internal data bus, the FFT microprocessor system, the transceiver between the TMS320 microprocessor and the internal data bus, and both interrupt circuits. If this test passes you know that the CPU can talk to the FFT microprocessor and the FFT microprocessor can interpret commands and respond (talk)to the system CPU.

FFT Interrupt Test This test checks the ability of the FFT board to interrupt the main system CPU and exercises the addressing and global bus circuits. The CPU interrupt must occur within a limited time. Two results are listed if this test is successful: the timeout test(called the "interrupt Registered" results) and the exercise routine results (called the"FFT Interrupt" results). The test runs as follows:

1. The system CPU (A2) loads a command into a register on the FFT board and starts a timer.

   This action utilizes the system bus interface circuits and the FFT interrupt circuit on the FFT board.

2. The FFT microprocessor system interprets the command, stores two numbers (5555H and AAAAH) in the scale factor registers in global RAM and activates the CPU interrupt.

   This action utilizes the FFT addressing circuitry, the global bus address and data interface circuits, and the CPU interrupt circuit on the FFT board.

3. If the system CPU receives the interrupt from the FFT board before the end of the timer cycle, the"FFT Interrupt Registered" test passes.
4. The CPU checks the numbers stored in RAM against a known number. If the numbers are identical, the"FFT Interrupt" test passes.

FFT RAM Test This test is a self-test run by the TMS320 FFT microprocessor on its own internal RAM. The test program resides in ROM in the FFT microprocessor system. The system CPU addresses the FFT board and loads a command to run the RAM test. After the test is complete the FFT board interrupts the system CPU and passes the test results (pass or fail) back to the CPU.

The system interface and both the FFT and CPU interrupt circuits are exercised as a byproduct of this test.

FFT ROM Test Each of the program and coefficient ROMs have a checksum number in the last byte. When the ROM test is run the system CPU reads the ROMs, generates its own checksum and compares it with the checksum stored in the program and coefficient ROMs.

To read the contents of the FFT ROMs, the CPU sends instructions to the FFT board causing it to place the ROM contents, one word at a time, into a specific location in global RAM where the CPU can access the data. The FFT board changes contents of another location of global RAM to zero each time it completes the transfer of a word. The CPU monitors this second location for an indication of valid data in the first location.

The system and global interface blocks are exercised as a by-product of this test.

Global Interface Test This tests moves (copies) a block of data from one area of global RAM to another area. It exercises both interrupt circuits and the address circuitry besides testing the global interface circuits.

The CPU instructs the FFT to do a block move, waits for the FFT to signal that it has finished the process, and then compares values of the two areas of RAM to determine whether the data copied is identical to the original data.

FFT Signature Analysis Tests

There are three digital signature tests designed to test the digital circuits on the FFT board. These tests are referred to by number as FFT Signature Analysis Test ONE, Test TWO, and Test THREE.

Test ONE tests the program ROMs (U301 and U303) and, to a limited extent, the TMS320 microprocessor. See table 8-22 for the signatures of Test ONE. With J3 and J4 in the test position (marked with a"T") the ROM output lines are disconnected and the TMS320 data lines are grounded. This test may be used to test the input and output signals of the ROM integrated circuits. The operation of the microprocessor is partially verified by this test because the address line outputs of the TMS320 are identical to the ROM input lines.

Test TWO may be used to test most of the circuits on the FFT board. The only exceptions are the global bus interface circuits. These require a special clock and are covered in Test THREE.

Test THREE may be used to test the global bus interface circuits (U511 through U516) and the coefficient ROM outputs (U315 and U317). This test uses the memory grant signal on test point 3 as a clock. See the table 8-26 for the signatures of Test THREE.

FFT Signature Analyzer Test ONE

1. Disconnect the power cable.
2. Put the FFT board on an extender card. All jumpers should be in the normal (N) position.
3. Connect and configure the signature analyzer as described in table 8-21.
4. Connect the power cable and turn ON power.

Table 8-21. FFT Signature Analyzer Setup ONE

Signal	Polarity	Connection
Ground	—	A9 J5-1
Clock	Neg edge	A9 J5-3
Stop	Neg edge	A9 J5-4
Start	Pos edge	A9 J5-5

5. Move Jumpers J3 and J4 to the test (T) position.
6. Move jumper J1 to the TST2 position.
7. Press the reset switch on the CPU board (A2 S1).
8. When completed, return all jumpers to the normal (N) position (either position OK for J1).

Note Steps 5, 6, and 7 activate the test.

Table 8-22. FFT Signature Analysis Test ONE

Component	Pin	Signature	Component	Pin	Signature
U301 and U303 address (input) lines	8	H62U	U303 only; data (output) lines	9	366P
	7	C21A		10	2UFH
	6	HA07		11	F7A2
	5	H0AA		13	0510
	4	P030		14	0637
	3	4442		15	2AA9
	2	4U2A		16	CAPA
	1	0772		17	0442
	23	9635			
	22	1734			
	21	8P54			
U301 only; data (output) lines	9	8551			
	10	91C0			
	11	3C0C			
	13	U6H7			
	14	6P56			
	15	29C5			
	16	CFPC			
	17	A484			

Return all jumpers to the normal (N) position (either position OK for J1).

FFT Signature Analysis Test TWO

1. Disconnect the power cable.
2. Put the FFT board on an extender card. All jumpers should be in the normal (N) position.
3. Connect and configure the signature analyzer as described in table 8-23.
4. Connect the power cable and turn ON power.

Table 8-23. FFT Signature Analyzer Setup TWO

Signal	Polarity	Connection
Ground	—	A9 J5-1
Clock	Neg edge	A9 J5-3
Stop	Neg edge	A9 J5-4
Start	Pos edge	A9 J5-5

5. Move jumper J2 to the test (T) position.
6. Move jumper J1 to the TST1 position.
7. Press the reset switch on the CPU board (A2 Sl). Allow ≅ 2 minutes for signatures to stabilize before checking.
8. When completed, return all jumpers to the normal (N) position (either position OK for J1).

Note Steps 5, 6, and 7 activate the test.

Table 8-24. FFT Signature Analysis Test TWO

Signal name	IC (pin)	Signature
TMS320 data lines:		
D0	U103(26)	31HP
D1	(25)	F8F2
D2	(24)	06F0
D3	(23)	001P
D4	(22)	U7P8
D5	(21)	5204
D6	(20)	0746
D7	(19)	1180
D8	(11)	9376
D9	(12)	P682
D10	(13)	349C
D11	(14)	053U
D12	(15)	UA51
D13	(16)	HPH7
D14	(17)	F091
D15	(18)	77HP
Internal data bus:		
IDB0	U503(18)	31HP
IDB1	(14)	F8F2
IDB2	(16)	06F0
IDB3	(17)	001P
IDB4	(15)	U7P8
IDB5	(11)	5204
IDB6	(13)	0746
IDB7	(12)	1180
IDB8	U403(18)	9376
IDB9	(17)	P682
IDB10	(16)	349C
IDB11	(15)	053U
IDB12	(14)	UA51
IDB13	(13)	HPH7
IDB14	(12)	F091
IDB15	(11)	77HP
Port decoder inputs.		
	U216(1)	1894
	(2)	0806
	(3)	9721
	(6)	P23A
	(4)	A712
	(5)	3P7P
	U217(1)	1894
	(2)	0806
	(3)	9271
	(6)	P23A
	(4)	0865
Port decoder outputs:		
SIRQSYSL	U216(15)	P23A
GDBOUTL	(14)	0HPC
	(13)	29FF
SDBUSOUTL	(12)	P23A
LDHWCRL	(11)	0807
LDCTR2L	(10)	5P63
LDPGSL	(9)	PC2U
	(7)	P23A
RIRQSYSL	U217(15)	P23A
GDBINL	(14)	2465
PROMINL	(13)	9CAU
SDBUSINL	(12)	P23A
SABUSINL		(11)
		(10)
CLRSCALEL		(9)
BFSUBADL		(7)

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature
I/O Sequencer:		
SEQSEL0	U117(9)	0CA9
SEQSEL10	(8)	A107
REALDATA	(7)	0C03
TWOCH	(6)	171A
GDINEMPTY	(5)	6476
GDOUTRDY	(5)	PUH1
PASSDONE	(3)	6052
DIDONE	(2)	A7C1
FFTMR	(27)	*
FFTMG	(26)	*
WINLOC	(25)	703P
PASSBIT0	(22,10)	14AA
CTRIENL	(21,13)	4P0A
	(20)	P23A
	(1)	0000
	(19)	PA3H
WINDPGL	(17)	FU43
FFTWR	(16)	9758
POSTINCL	(15)	15FU
REQGBL	(12)	3176
LDCAL	(11)	3H40
Sequence decoder:		
SEQSEL1	U115(1)	A107
SEQSEL0	(2)	0AC9
CTR2DNL	(3)	8C22
CTRIENL	(4)	4P0A
POSTINCL	(5)	15FU
CLKOUTL	(6)	0000
REQGBL	(7)	3176
FFTWR	(8)	9758
CTRB11	(9)	80UA
W11	(11)	2U78
CLRRDYL	(19)	P8P0
CLREMPTYL	(18)	7228
FA11	(17)	H351
INC1L	(15)	4348
DEC2L	(14)	U42A
INC2L	(13)	A2AH

Signal name	IC (pin)	Signature
Hardware Control Registers:		
IDB15	U406(2)	77HP
IDB14	(3)	F091
IDB13	(4)	HPH7
IDB12	(5)	UA51
IDB11	(6)	053U
IDB10	(7)	349C
IDB9	(8)	P682
IDB8	(9)	9376
LDHWCRL	(11)	0807
WINLOC	(19)	703P
BNKSEL	(18)	AAF4
SWAP	(17)	P41A
CTR2DNL	(16)	8C22
TWOCH	(15)	171A
REALDATA	(14)	0C09
SEQSEL1	(13)	A107
SEQSEL0	(12)	0AC9
IDB7	U405(2)	1180
IDB6	(3)	0746
IDB5	(4)	5204
IDB4	(5)	U7P8
IDB2	(7)	06F0
IDB3	(6)	001P
IDB1	(8)	F8F2
IDB0	(9)	31HP
LDHWCRL	(11)	0807
LEV2	(19)	PACU
LEV1	(18)	F167
LEV0	(17)	H441
TBSEL2	(16)	F789
TBSEL1	(15)	815H
TBSEL0	(14)	3A50
SCALE1	(13)	C1CP
SCALE0	(12)	8H36

* use Test Three for signatures of these signals

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature	Signal name	IC (pin)	Signature
Pseudo Scale:			Global Address Bus Interface:		
IDB8	U305(5)	9376	FA15	U512(2)	9993
IDB9	(6)	P682	FA14	(3)	2088
IDB10	(7)	349C	FA13	(4)	3FU7
IDB11	(4)	053U	FA12	(5)	08P8
IDB12	(3)	UA51	FA11	(6)	H351
1DB13	(2)	HPH7	FA10	(7)	6739
IDB14	(1)	F091	FA9	(8)	1P6P
IDB15	(15)	77HP	FA8	(9)	C904
	(12)	8090	REQGBL	(11)	3176
	(11)	54H8	FA7	U511(2)	5C91
CLRSCALEL	U208(5,11)	AH5F	FA6	(3)	H289
GDBOUTL	(4,12)	0HPC	FA5	(4)	F6C8
DIVBY4	(7)	1384	FA4	(5)	444H
DIVBY2	(9)	H4UC	FA3	(6)	85PP
Pseudorandom Number Generator:			FA2	(7)	46C7
CLRPRNL	U105(9)	PLHF	FA1	(8)	7H94
GDBOUTL	(12)	0HPC	FA0	(9)	4282
	(11)	284A	Global Data Bus Interface:		
PRN	(14)	5828	IDB15	U516(2), U515(19)	77HP
	U106(11)	8H75	IDB14	U516(3), U515(18)	F091
	(5)	21U9	IDB13	U516(4), U515(17)	HPH7
	U107(11)	5H4P	IDB12	U516(5), U515(16)	UA51
	U108(11)	F61F	IDB11	U516(6), U515(15)	053U
	U108(4)	PC89	IDB10	U516(7), U515(14)	349C
	U408(11)	FA70	IDB9	U516(8), U515(13)	P682
Test Bit Mux:			IDB8	U516(9), U515(12)	9376
DIVBY4	U206(2)	1384	IDB7	U514(2), U513(19)	1180
DIVBY2	(1)	H4UC	IDB6	U514(3), U513(18)	9746
PASSDONE	(15)	6052	IDB5	U514(4), U513(17)	5204
PRN	(13)	5828	IDB4	U514(5), U513(16)	U7P8
	(5)	6506	IDB3	U514(6), U513(15)	001P
			IDB2	U514(7), U513(14)	06F0
			IDB1	U514(8), U513(13)	F8F2
			IDB0	U514(9), U513(12)	31HP

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature
Counter One:		
	U209(13)	UU11
	(12)	0CA2
	(11)	A172
LDCTR2L	(10)	5P63
PASSDONE	(3)	6052
DIDONE	(2)	A7C1
	(1)	A512
	(15)	U9F5
	U210(13)	UU11
	(11)	A172
LDCTR2L	(10)	5P63
	(9)	0CA2
	(7)	9580
	(6)	C207
	(5)	859C
	(4)	6530
	(3)	P490
	(2)	A634
	(1)	4048
	(15)	60H1
Counter Two:		
IDB11	U411(9)	053U
IDB10	(10)	349C
IDB9	(1)	P682
IDB8	(15)	9376
LDCTR2L	(11)	5P63
	(4)	CPH4
	(5)	PP8P
	(13)	3044
	(12)	9PAC
	(7)	80UA
	(6)	4673
	(2)	3800
	(3)	6H0A
IDB7	U410(9)	1180
IDB6	(10)	0746
IDB5	(1)	5204
Counter Two Continued:		
IDB4	(15)	U7P8
LDCTR2L	(11)	5P63
	(4)	21AP
	(5)	3HA8
	(13)	CPH4
	(12)	PP8P
	(7)	5603
	(6)	U4C2
	(2)	662A
	(3)	83C6
IDB3	U409(9)	001P
IDB2	(10)	06F0
IDB1	(1)	F8F2
IDB0	(15)	31HP
LDCTR2L	(11)	5P63
DEC2L	(4)	U42A
INC2L	(5)	A2AH
	(13)	21AP
	(12)	3HA8
	(7)	UAH2
	(6)	9AC9
	(2)	2813
	(3)	FH82

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature	Signal name	IC (pin)	Signature
Counter MUX:			Butterfly Type PLA (U207):		
DIDONE	U311(5)	A7C1		U207(1)	A7C1
	(11)	A512		(2)	A512
	(14)	U9F5		(3)	U9F5
	(6)	4673		(4)	9580
	(10)	3800		(5)	C207
	(13)	6H0A		(6)	859C
ACB10	(7)	7U15		(7)	6530
ACB9	(9)	7FA4		(8)	P490
ACB8	(12)	A033	LEV0	(9)	H441
CTR1ENL	(1)	4P0A	LEV1	(11)	F167
	U310(2)	9580	LEV2	(12)	PACU
	(5)	C207	TYPE2BF	(15)	44CP
	(11)	859C	Butterfly Subroutine Address ROM:		
	(14)	6530	SCALE0	U502(10)	8H36
	(3)	5603	SCALE1	(11)	C1CP
	(6)	U4C2	PASSDONE	(12)	6052
	(10)	662A	TYPE2BF	(13)	44CP
	(13)	83C6	BFSUBADL	(15)	U8F9
ACB7	(4)	86H2	IDB0	(1)	31HP
ACB6	(7)	0169	IDB1	(2)	F8F2
ACB5	(9)	0CH4	IDB2	(3)	06F0
ACB4	(12)	0152	IDB3	(4)	001P
CTR1ENL	(1)	4P0A	IDB4	(5)	U7P8
	U309(2)	P490	IDB5	(6)	5204
	(5)	A634	IDB6	(7)	0756
	(11)	4048	IDB7	(9)	1180
	(14)	60H1			
	(3)	UAH2			
	(6)	9AC9			
	(10)	2813			
	(13)	FH82			
ACB7	(4)	349A			
ACB6	(7)	6AH1			
ACB5	(9)	1U59			
ACB4	(12)	4282			
CTR1ENL	(1)	4P0A			
(ACB is address count bus)					

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature	Signal name	IC (pin)	Signature
Address Translator:			Coefficient ROM:		
FFTWR	U307(4)	9758	FA0	U412(2)	4282
SWAP	(5)	P41A	FA1	(3)	7H94
	(6)	A7C3	FA2	(4)	46C7
ACB2	U314(1)	6AH1	FA3	(5)	85PP
ACB4	(2)	0152	FA4	(6)	444H
ACB6	(3)	0169	FA5	(7)	F6C8
ACB8	(4)	A033		(19)	1411
	(5)	H8A6		(18)	2277
LEV0	(6)	H441		(17)	1683
LEV1	(7)	F167		(16)	A57C
LEV2	(8)	PACU		(15)	U27A
WINDPGL	(9)	FU43		(14)	6C31
FFTWR	(11)	9758	FA6	U413(2)	H289
FA2	(19)	46C7	FA7	(3)	5C91
FA4	(18)	444H	FA8	(4)	CP04
FA6	(17)	H289	FA9	(5)	1P6P
FA8	(16)	C904	FA10	(6)	6739
FA10	(12)	6739	FA11	(7)	H351
ACB1	U313(1)	1U59	FA12	(8)	08P8
ACB3	(2)	349A	FA13	(9)	3FU7
ACB5	(3)	0CH4	LDCAL	(11)	3H40
ACB7	(4)	86H2		(19)	F186
ACB9	(5)	7FA4		(18)	PU20
FA1	(19)	7H94		(17)	2U40
FA3	(18)	85PP		(16)	6AHA
FA5	(17)	F6C8		(15)	47HH
FA7	(16)	5C91		(14)	H351
FA9	(12)	1P6P		(13)	08P8
ACB0	U307(12)	4282		U315(10), U317(10)	1411
PASSBIT0	(13)	14AA		U315(9), U317(9)	2277
FA0	(11)	4282		U315(8), U317(8)	1683
(ACB— is address count bus;				U315(7), U317(7)	A57C
FA— is FFT address bus)				U315(6), U317(6)	U27A
				U315(5), U317(5)	6C31
				U315(4), U317(4)	F186
				U315(3), U317(3)	PU29
				U315(25), U317(25)	2U40
				U315(24), U317(24)	6AHA
				U315(21), U317(21)	47HH
				U315(23), U317(23)	H351
				U315(2), U317(2)	08P8

FFT Signature Analysis Test TWO continued

Signal name	IC (pin)	Signature
Coefficient ROM continued:		
IDB0	U517(18)	31HP
IDB1	(17)	F8F2
IDB2	(16)	06F0
IDB3	(15)	001P
IDB4	(14)	U7P8
IDB5	(13)	5204
IDB6	(12)	0746
IDB7	(11)	1180
IDB8	U518(18)	9376
IDB9	(17)	P682
IDB10	(16)	349C
IDB11	(15)	053U
IDB12	(14)	UA51
IDB13	(13)	HPH7
IDB14	(12)	F091
IDB15	(11)	77HP

Return all jumpers to the normal (N) position (either position OK for J1).

FFT Signature Analysis Test THREE

1. Disconnect the power cable.
2. Put the FFT board on an extender card. All jumpers should be in the normal (N) position.
3. Connect the power cable and turn ON power.
4. Connect the signature analyzer as described in table 8-25.

Table 8-25. FFT Signature Analyzer Setup THREE

Signal	Polarity	Connection
Ground	—	A9 J5-1
Clock	Pos edge*	A9 TP3*
Stop	Neg edge	A9 J5-4
Start	Pos edge	A9 J5-5

* note change from Test Two

5. Move jumper J2 to the test (T) position.
6. Move jumper J1 to the TST1 position.
7. Press the reset switch on the CPU board (A2 S1).
8. When completed, return all jumpers to the normal (N) position (either position OK for J1).

Note

Steps 5, 6, and 7 activate the test.

Table 8-26. FFT Signature Analysis Test THREE

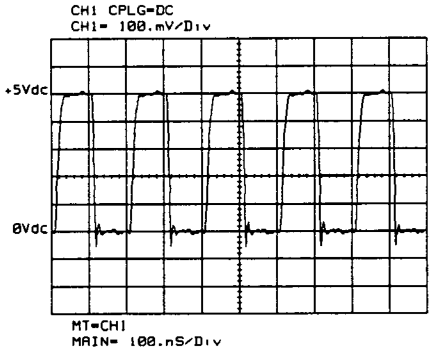
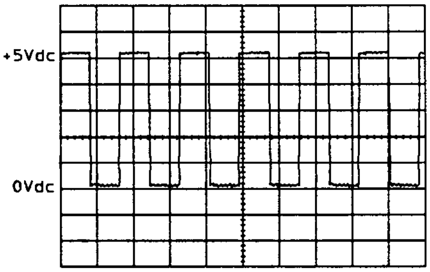
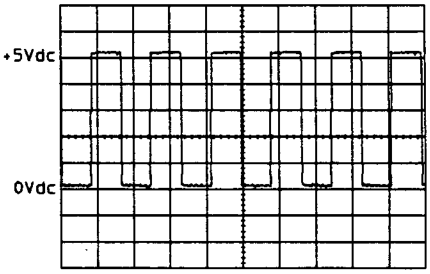
Signal name	IC (pin)	Signature	Signal name	IC (pin)	Signature
	U315(11), U517(2)	47FP	Global Data Bus Interface Outputs:		
	U315(12), U517(3)	3246	GD15L	U516(19), U515(2)	3347
	U315(13), U517(4)	HA4U	GD14L	U516(18), U515(3)	U9FH
	U315(15), U517(5)	903F	GD13L	U516(17), U515(4)	3347
	U315(16), U517(6)	AP58	GD12L	U516(16), U515(5)	U9FH
	U315(17), U517(7)	0011	GD11L	U516(15), U515(6)	3347
	U315(18), U517(8)	C668	GD10L	U516(14), U515(7)	U9FH
	U315(19), U517(9)	3F07	GD9L	U516(13), U515(8)	3347
	U317(11), U518(2)	6P1C	GD8L	U516(12), U515(9)	U9FH
	U317(12), U518(3)	P0HU	GD7L	U514(19), U513(2)	3347
	U317(13), U518(4)	CC3C	GD6L	U514(18), U513(3)	U9FH
	U317(15), U518(5)	4472	GD5L	U514(17), U513(4)	3347
	U317(16), U518(6)	PHH1	GD4L	U514(16), U513(5)	U9FH
	U317(17), U518(7)	0HHA	GD3L	U514(15), U513(6)	3347
	U317(18), U518(8)	H231	GD2L	U514(14), U513(7)	U9FH
	U317(19), U518(9)	0HP6	GD1L	U514(13), U513(8)	3347
PROMINL	U517(1), U518(1)	FA8A	GD0L	U514(12), U513(9)	U9FH
Global Address Bus Interface Outputs:			Handshake:		
GA16L	U512(19)	3347	FFTMG	U212(12)	F59A
GA15L	(18)	18C1		(13)	FA8A
GA14L	(17)	4UAU		(11)	0U10
GA13L	(16)	7FH4	FFTMR	U211(12,13)	0000
GA12L	(15)	U839	FFTWR	U501(2)	F59A
GA11L	(14)	A440	REQGBL	(3)	FA8A
GA10L	(13)	4020	LDGDBRL	U214(3)	FA8A
GA9L	(12)	15PP	GR/GWL	U211(8)	0U10
GA8L	U511(19)	4PP9	MGFFTL	U215(13)	0000
GA7L	(18)	U5U7	GDSL	U214(2)	FA8A
GA6L	(17)	4291	MRFFTL	U211(11)	FA8A
GA5L	(16)	6F84			
GA4L	(15)	3831			
GA3L	(14)	A997			
GA2L	(13)	FF53			
GA1L	(12)	P39F			

Return all jumpers to the normal (N) position when testing is complete.

FFT Signal Waveforms

The following table of illustrations are oscilloscope plots of digital signature analysis signals (CLOCK and START/STOP) at J5. These should appear on the test pins when the SA jumpers are in the positions specified in the waveform setup.

Table 8-27. FFT Signal Waveforms

Setup	Parameters	Waveform
Jumpers in normal position		
CLKOUT (5 MHz) Signal at pin 3 of J5 (CLK on SA connector) Scale 1 V/div Timebase 100 ns/div Delta V 5 V Trigger Ch 1 Coupling dc	Time period and pulse shape	 **#1**
Put J2 in the test (T) position, J1 in the TST1 position and press the reset button on the CPU board (A2 S1).		
SRT/STP TST 1 (1.4 Hz) Signal at pin 4 and 5 of J5 (SA connector) Scale 1 V/div Timebase 500 ms/div Delta V 5V Trigger Ch 1 Coupling dc	Time period and pulse shape	 **#2**
Put J3 and J4 in the test position and J1 in the TST2 position		
SRT/STP TST 2 (1.2 kHz) Signal at pins 4 and 5 of J5 (DSA connector) Scale 1 V/div Timebase 500 us/div Delta V 5V Trigger Ch1 Coupling dc	Time period and pulse shape	 **#3**

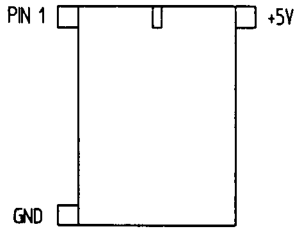
FFT After-Repair Adjustments and Tests

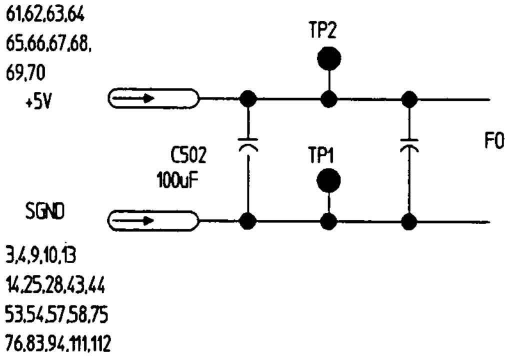
Table 8-28. After-Repair Adjustments and Tests

Perform the following:*	Section
Diagnostic Tests: Test All	VII
Adjustments: None	—
Performance Tests: None	—

*Return all jumpers to the normal (N) position.

ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED

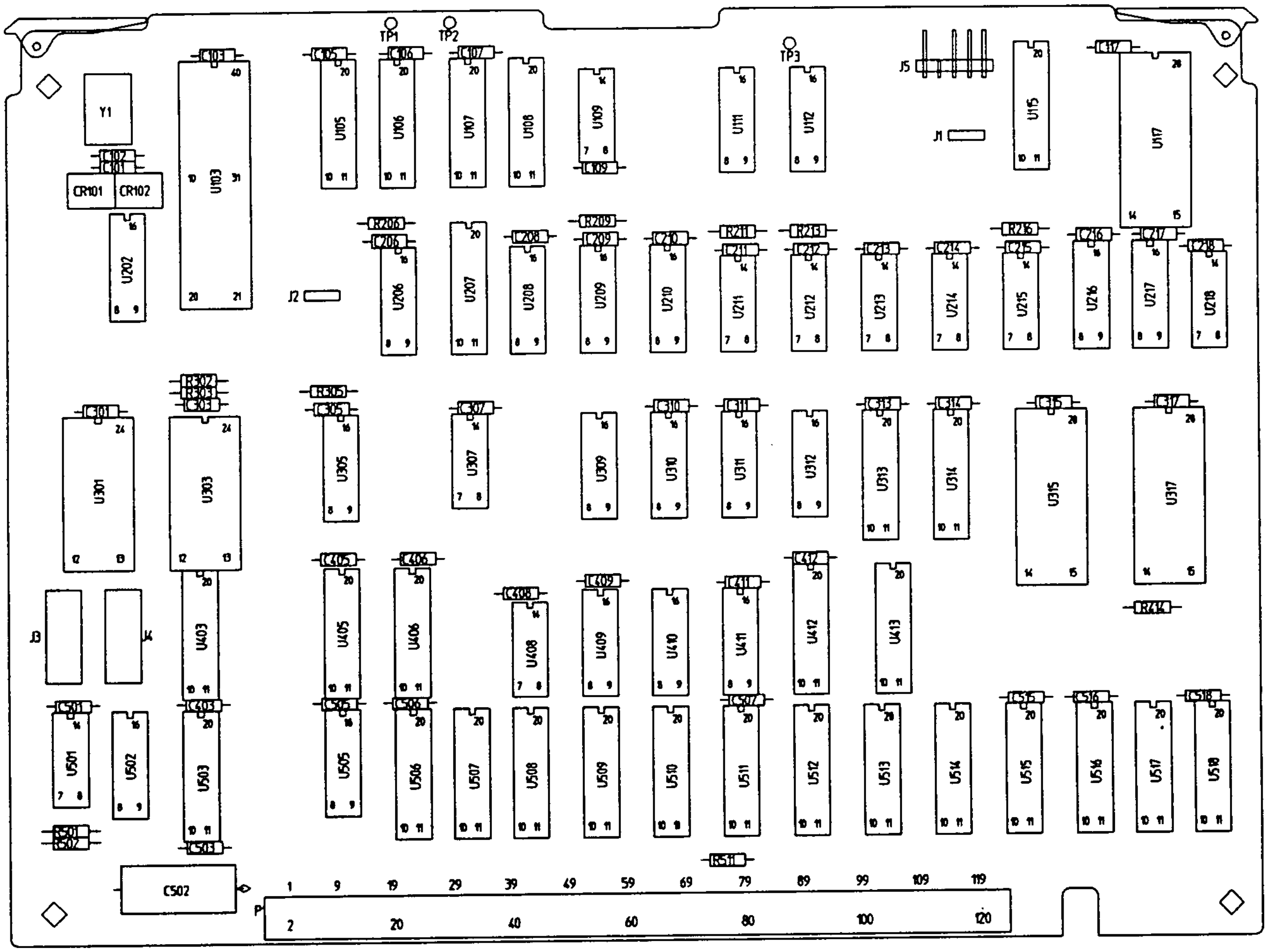




FOR ALL BYPASS CAPS

C103 C105 C106 C107 C109
C117 C206 C208 C209 C210
C211 C212 C213 C214 C215
C218 C217 C218 C301 C303
C305 C307 C310 C311 C313
C314 C315 C317 C403 C405
C406 C409 C409 C411 C412
C501 C503 C505 C506 C507
C515 C516 C518

A9 Fast Fourier Transform (FFT) Processor Ground and Power Chart
P/N 03562-66509 Rev B



A9 Fast Fourier Transform (FFT) Processor Component Locator

P/N 03562-66509 Rev B

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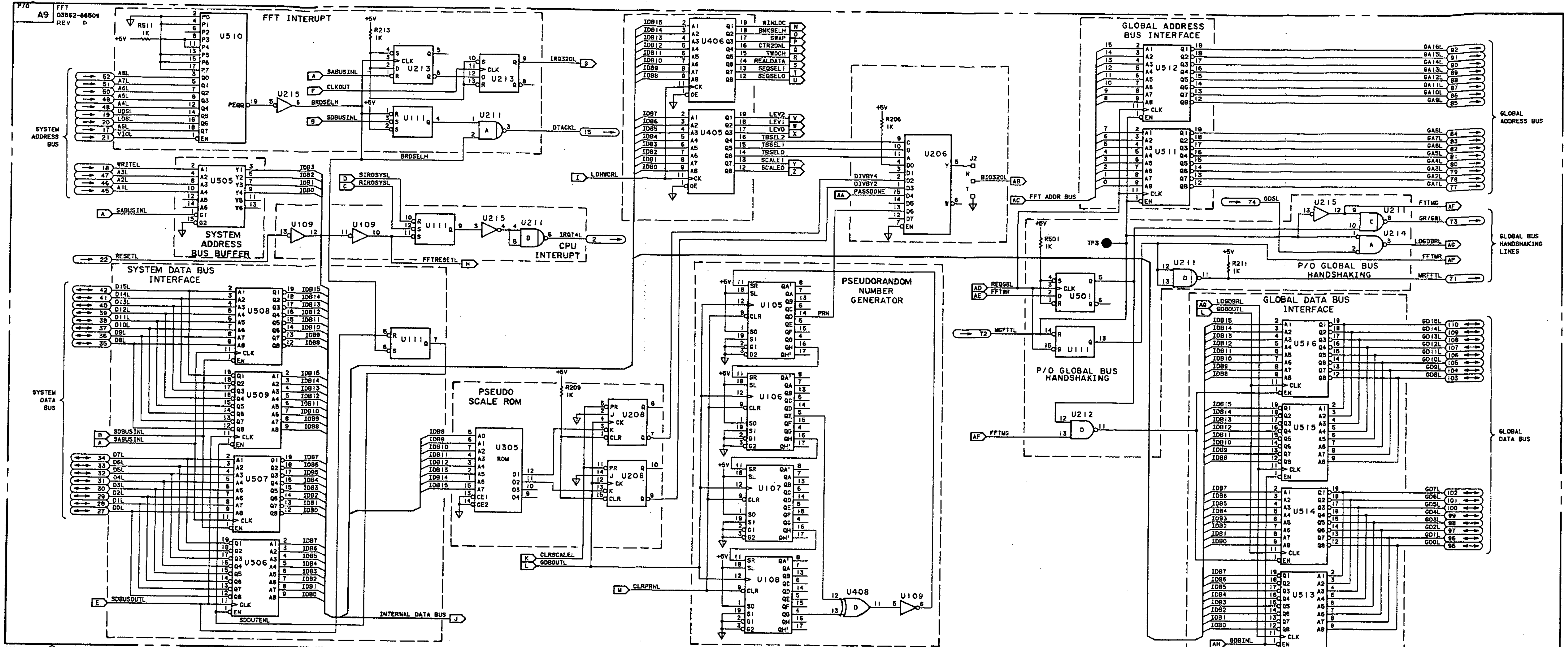

A9 Fast Fourier Transform (FFT) Processor Schematic
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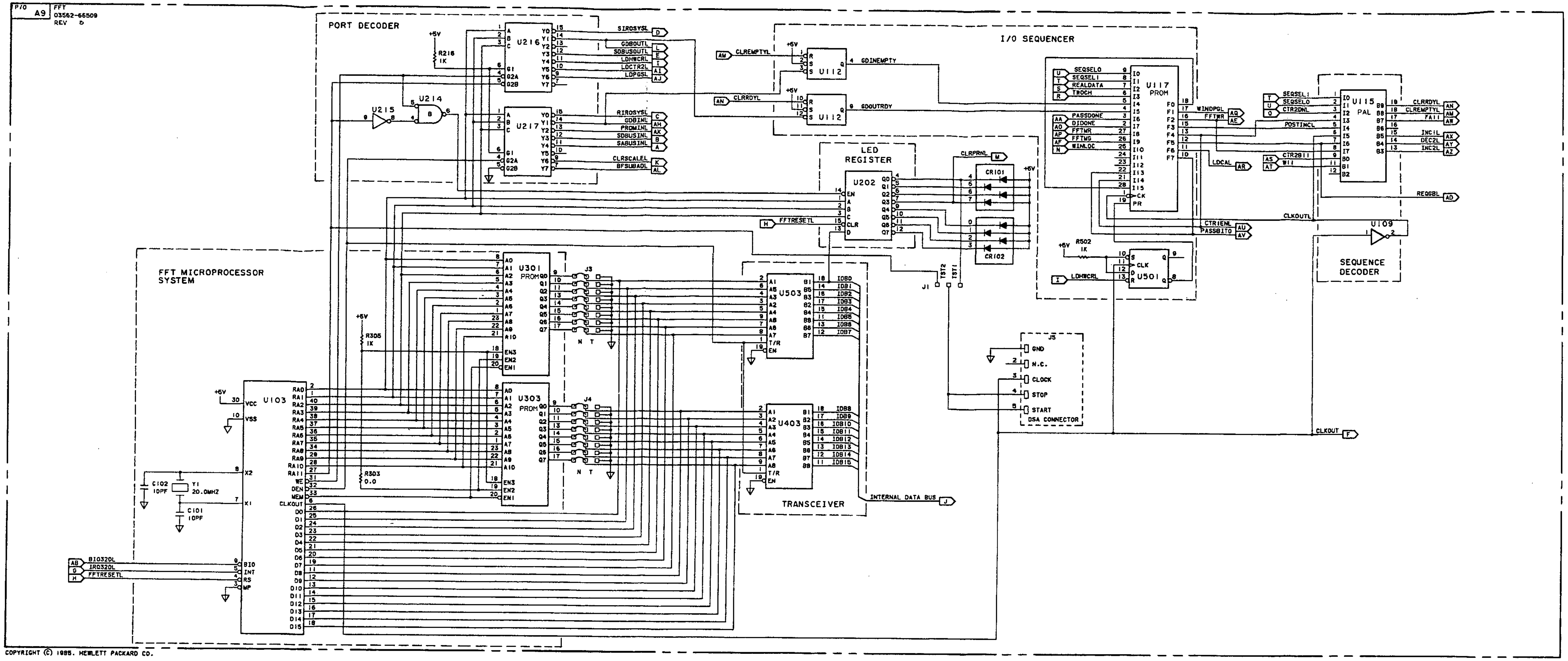

A9 Fast Fourier Transform (FFT) Processor Schematic
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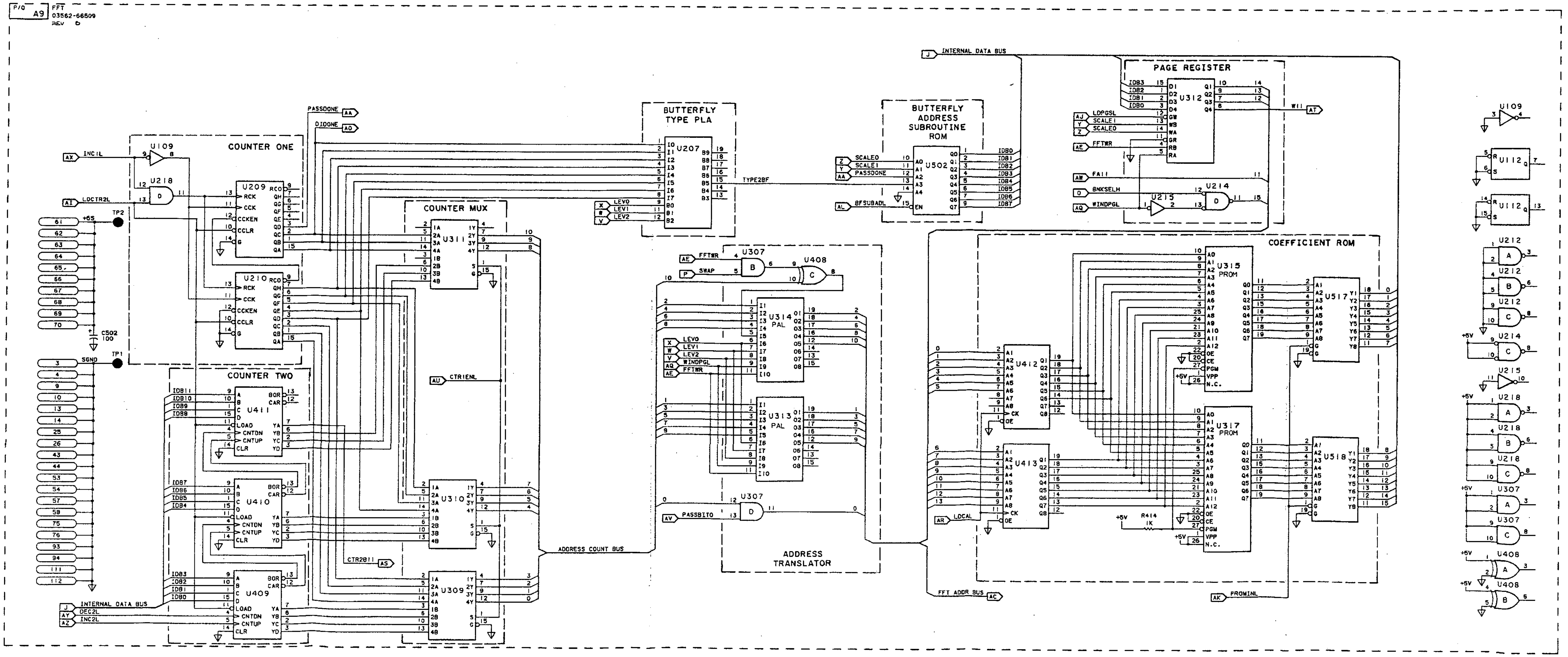

A9 Fast Fourier Transform (FFT) Processor Schematic
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A14
Mother Board

A14 Mother Board

The information in this section should be used to trace the interconnecting signals between the HP 3563A assemblies. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the Circuit Descriptions of Section VI are understood.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Caution Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

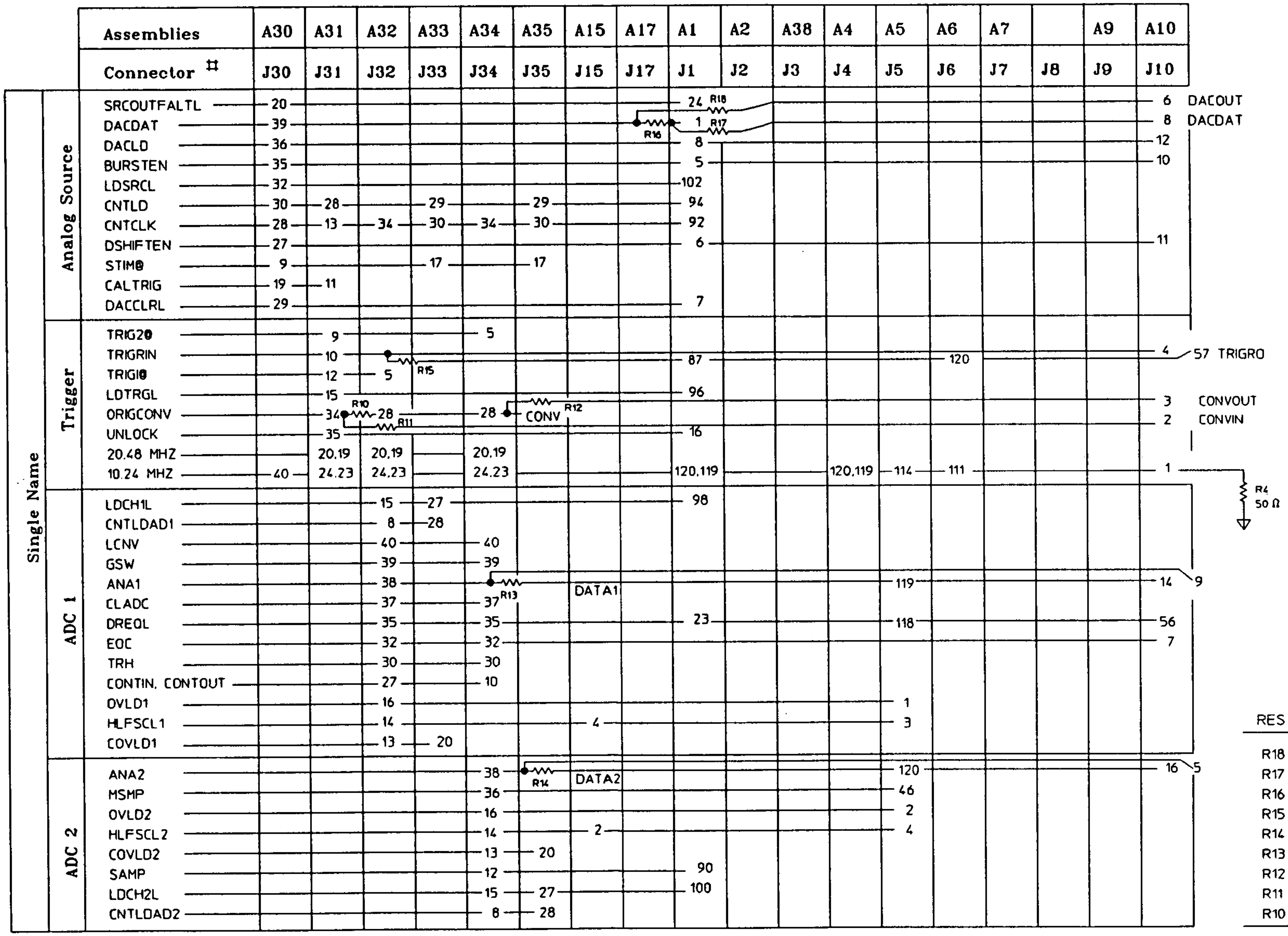
How to Use This Section

Start Table 8-29 lists all the inter-assembly signal connections. The signal names are listed vertically. The assembly designators and connector numbers are listed horizontally. When a signal is connected to an assembly, the edge connector pin number is entered in the table at the intersection point of the signal name and the assembly in the matrix.
For example:

Pin Number →	13	15
	Signal Origin (Shown in bold)	Signal Destination

Reference The component locator follows table 8-29. For the location of cables and boards refer to figure 4-1 in Section IV.

Table 8-29. Control and Interconnecting Signals

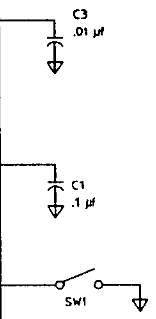


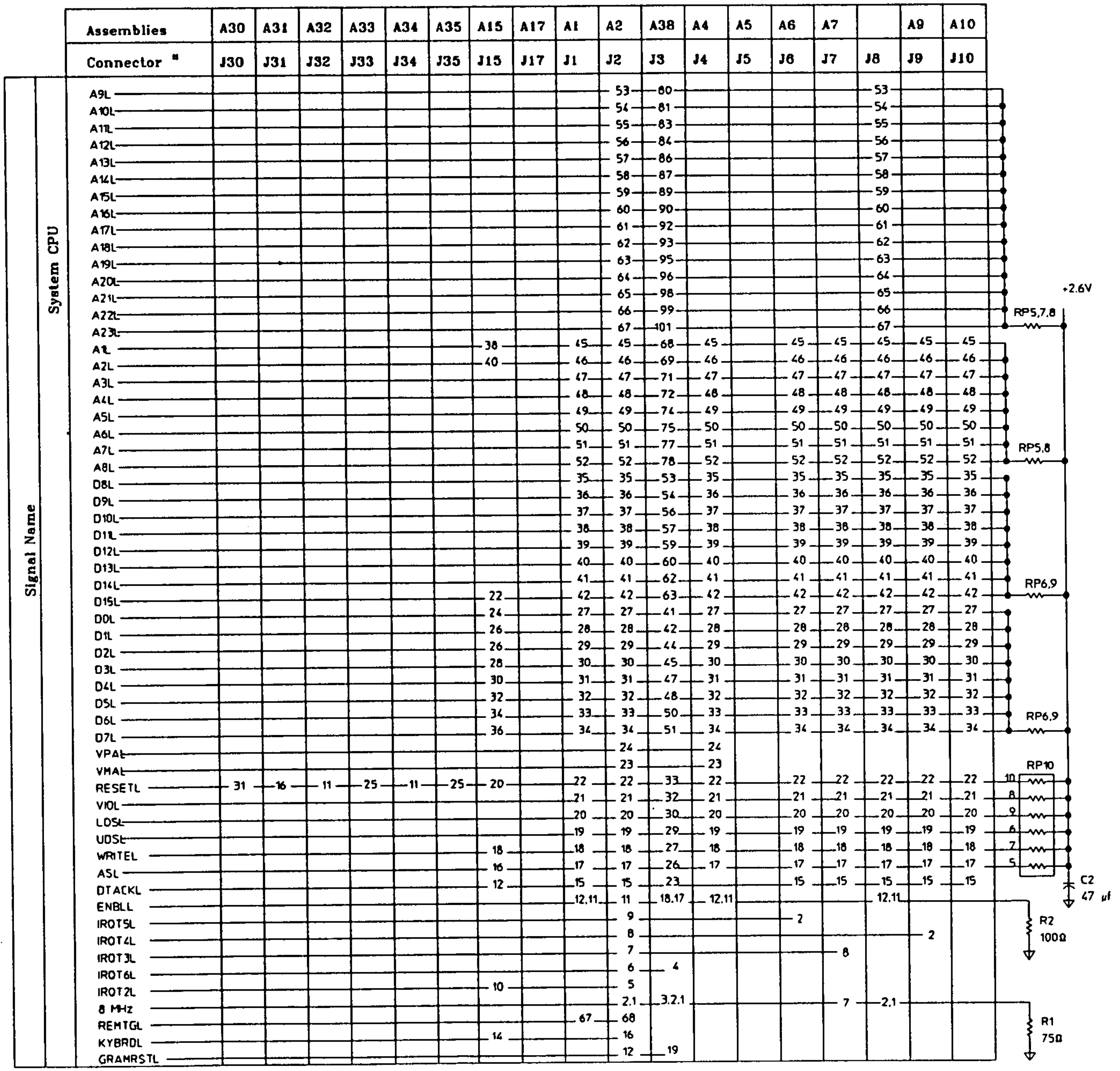
Single Name	Assemblies	A30	A31	A32	A33	A34	A35	A15	A17	A1	A2	A38	A4	A5	A6	A7		A9	A10
	Connector ⌗	J30	J31	J32	J33	J34	J35	J15	J17	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
Analog Source	SRCOUTFALTL	20								24 R18									6 DACOUT
	DACDAT	39							R16	1 R17									8 DACDAT
	DACLD	36								8									12
	BURSTEN	35								5									10
	LDSRCL	32								102									
	CNTLD	30	28		29		29			94									
	CNTCLK	28	13	34	30	34	30			92									
	DSHIFTEN	27								6									11
	STIM0	9			17		17												
	CALTRIG	19	11																
	DACCLRL	29								7									
Trigger	TRIG20		9			5													
	TRIGRIN		10	R15						87					120				4 57 TRIGRO
	TRIGI0		12	5															
	LDTRGL		15							96									3 CONVOUT
	ORIGCONV		34 R10	28 R11		28	CONV R12												2 CONVIN
	UNLOCK		35							16									
	20.48 MHZ		20,19	20,19		20,19													
	10.24 MHZ	40	24,23	24,23		24,23				120,119			120,119	114	111				1 R4 50 Ω
ADC 1	LDCH1L			15	27					98									
	CNTLDAD1			8	28														
	LCNV			40		40													
	GSW			39		39													
	ANA1			38		R13		DATA1						119					14 9
	CLADC			37		37													
	DREQL			35		35				23				118					56
	EOC			32		32													7
	TRH			30		30													
	CONTIN, CONTOUT			27		10													
	OVLD1			16										1					
	HLFSCL1			14				4						3					
	COVLD1			13	20														
ADC 2	ANA2					38	R14	DATA2						120					16 5
	MSMP					36								46					
	OVLD2					16								2					
	HLFSCL2					14		2						4					
	COVLD2					13	20												
	SAMP					12				90									
	LDCH2L					15	27			100									
	CNTLDAD2					8	28												

RES	PRODUCT
R18	HP 3563
R17	HP 3563
R16	HP 3562
R15	HP 3562
R14	HP 3562
R13	HP 3562
R12	HP 3563
R11	HP 3563
R10	HP 3562

Control and Interconnecting Signals continued

Signal Name	Assemblies	A30	A31	A32	A33	A34	A35	A15	A15	A17		A1	A2	A38	A4	A5	A6	A7		A9	A10
	Connector #	J30	J31	J32	J33	J34	J35	J15	J16	J17	J18	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
Power Supply	+5S (W22)	26,25, 24,23	40,39, 38,37						1	1,2,3		64,63,62 61,60,59, 58,57	116,115, 114,113, 112,111	189,188, 186,185, 183,182, 177,176, 174,173, 168,167, 128,125, 122,119, 116,114, 113	70,69,68 67,66,65 64,63,62 61,60,59, 58,57	12,11,10, 9,8,7	12,11,10, 9,8,7	120,119, 118,117, 116,115, 114,113, 112,111, 68,67,66 65,64,63 62,61,60, 59	10,9,8, 7,6,5, 4,3	70,69,68 67,66,65 64,63,62 61,60,59	86,85,84, 83,82,81, 80,79,78 77,76,75
	-5V										3										113-120
	+30V				8,10		8,10														
	-30V				2,4		2,4														
	+15A	13-16	7,8	7,9	7,9	7,9	7,9														
	-15A	1-4	5,6	1,3	1,3	1,3	1,3														
	+5 FNTEND			2,4,6	23,21, 14,13	2,4,6	23,21, 14,13														
	+26V	To Termination Networks																			
	+8S1															112					
	+8S2															111					
	+15S											114,113	119			48					
	-15S											110,109	120			47					
	OTEMP										1										
	PWRDNL	37											118								
	PWRUP												117								
	SMPOUT		29																		
	SGND(W23)	38,33,22 21,18,17, 12,11,10, 8,7,6,5	36,32,31, 30,27,26 25,22,21, 18,17,4, 3,2,1	33,31,29, 26,25,22 21,18,17	26,24,22 19,15,12, 11,6,5	33,31,29, 26,25,22 21,18,17,	26,24,22 19,15,12, 11,6,5	1-39 odd 8 (conectl)	2	5-39 odd	2	118,117, 112,111, 97,93,86 85,82,81, 78,77,74 73,70,69 54,53,44 43,26,25 14,13,10, 9,4,3	94,93,76 75,70,69 44,43,26 25,14,13, 10,4,3	187,184, 181,180, 179,178, 175,172, 171,170, 169,166, 163,160, 157,154, 151,148, 145,141, 140,136, 133,130, 108,107, 105,104, 102,73,70 67,66,65, 64,61,58, 55,52,49, 46,43,40, 39,38,37, 36,35,34, 31,28,25, 22,21,20, 15,14,13, 12,11,10, 9,8,7,6,5	118,117, 114,113, 112,111, 110,109, 108,107, 106,105, 102,101, 100,99, 98,97,96 95,94,93 90,89,88 87,86,85 82,81,78, 77,74,73 54,53,44 43,26,25 14,13,10, 9,4,3	116,115, 94,93,76, 75,68,67, 50,49,32, 31,18,17	118,117, 114,113, 110,109, 106,105, 104,103, 86,85,68, 67,54,53, 44,43,26, 25,4,3	94,93,76, 75,72,71, 58,57,56, 55,54,53, 44,43,26, 25,14,13, 12,11,10, 9,6,5,4, 3,2,1,	118,117, 116,115, 114,113, 112,111, 94,93,76, 75,44,43, 26,25,24, 14,13	120,119, 116,115, 112,111, 94,93,76 75,58,57 54,53,44 43,26,25 14,13,10, 9,4,3	108,107, 106,105, 104,103, 102,101, 100,99,98, 97,96,95, 94,93,92, 72,71,70, 69,68,67, 66,65,64, 63,62,61, 44,43,26, 25,24,23





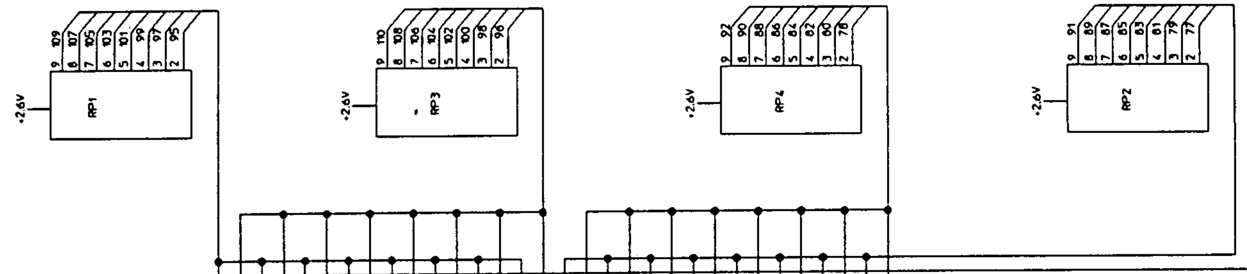
Signal Name

System CPU

Assemblies	A30	A31	A32	A33	A34	A35	A15	A17	A1	A2	A38	A4	A5	A6	A7		A9	A10
Connector *	J30	J31	J32	J33	J34	J35	J15	J17	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
A9L										53	80					53		
A10L										54	81					54		
A11L										55	83					55		
A12L										56	84					56		
A13L										57	86					57		
A14L										58	87					58		
A15L										59	89					59		
A16L										60	90					60		
A17L										61	92					61		
A18L										62	93					62		
A19L										63	95					63		
A20L										64	96					64		
A21L										65	98					65		
A22L										66	99					66		
A23L										67	101					67		
A1L							38		45	45	68	45		45	45	45	45	45
A2L							40		46	46	69	46		46	46	46	46	46
A3L									47	47	71	47		47	47	47	47	47
A4L									48	48	72	48		48	48	48	48	48
A5L									49	49	74	49		49	49	49	49	49
A6L									50	50	75	50		50	50	50	50	50
A7L									51	51	77	51		51	51	51	51	51
A8L									52	52	78	52		52	52	52	52	52
D8L									35	35	53	35		35	35	35	35	35
D9L									36	36	54	36		36	36	36	36	36
D10L									37	37	56	37		37	37	37	37	37
D11L									38	38	57	38		38	38	38	38	38
D12L									39	39	59	39		39	39	39	39	39
D13L									40	40	60	40		40	40	40	40	40
D14L									41	41	62	41		41	41	41	41	41
D15L							22		42	42	63	42		42	42	42	42	42
D0L							24		27	27	41	27		27	27	27	27	27
D1L							26		28	28	42	28		28	28	28	28	28
D2L							26		29	29	44	29		29	29	29	29	29
D3L							28		30	30	45	30		30	30	30	30	30
D4L							30		31	31	47	31		31	31	31	31	31
D5L							32		32	32	48	32		32	32	32	32	32
D6L							34		33	33	50	33		33	33	33	33	33
D7L							36		34	34	51	34		34	34	34	34	34
VPAL										24		24						
VMAL										23		23						
RESETL	31	16	11	25	11	25	20		22	22	33	22		22	22	22	22	22
VIOL									21	21	32	21		21	21	21	21	21
LDSL									20	20	30	20		20	20	20	20	20
UDSL									19	19	29	19		19	19	19	19	19
WRITEL							18		18	18	27	18		18	18	18	18	18
ASL							16		17	17	26	17		17	17	17	17	17
DTACKL							12		15	15	23			15	15	15	15	15
ENBLL									12,11	11	18,17	12,11				12,11		
IROT5L										9				2				
IROT4L										8							2	
IROT3L										7					8			
IROT6L										6	4							
IROT2L							10			5								
8 MHz										2,1	3,2,1				7	2,1		
REMTGL									67	68								
KYBRDL							14			16								
GRAMRSTL										12	19							

		Assemblies	A30	A31	A32	A33	A34	A35	A15	A17	A1	A2	A38	A4	A5	A6	A7		A9	A10
		Connector #	J30	J31	J32	J33	J34	J35	J15	J17	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
Signal Name	Digital Source	DACCLK	34								2									
		NSYNC									91			91						91
		BFST									84			84		116				55
		ARML									83					115				
		NDAT									80			80						
		NLD									79			79						
		NDCK									76			76						
		NCLK									75			75						
	Digital Filter	SYNC2												6.5	16.15	16				
		COS												2	6					
		SINE												1	5					
		LD0-LD15													51-66	87-102				
		CH2BG1L													42	78				
		CH1BG1L													40	76				
		BLK3FULL													39	75				
		BLK2FULL													38	74				
		SYSCLK													113	108				
		CH1STOP1													117	112				
		CH2STOP1													44	80				
		CH2BR1L													26	62				
		CH1BR1L													25	61				
	D Fltr Cont	INBLKEMPTY													36	72				
		BWRITEL													34	24				
		MCLK													33	69				
		BRESETL													30	23				
		CH2LOSEL													29	65				
		CH1LOSEL													45	66				
		FLTRST													28	64				
		DMADTACKL													24	60				
		MYADDASL													23	59				
		BA4L													22	58				
		BA3L													21	57				
		BA2L													20	56				
		BA1L													19	55				
		BLDSL													14	14				
		BUDSL													13	13				
		TRIGGER							6							119				
		UNUSED1													27	63				
		UNUSED2													28	64				
		UNUSED3													33	69				
		UNUSED4													35	71				
		UNUSED5													37	63				
		UNUSED6													41	77				
		UNUSED7													43	79				

Control and Interconnecting Signals continued



Assemblies	A30	A31	A32	A33	A34	A35	A15	A17	A1	A2	A38	A4	A5	A6	A7		A9	A10
Connector [a]	J30	J31	J32	J33	J34	J35	J15	J17	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
Signal Name Global RAM																		
GD0L								34		95	143		95		95	95	95	
GD1L								32		96	144		96		96	96	96	
GD2L								30		97	146		97		97	97	97	
GD3L								28		98	147		98		98	98	98	
GD4L								26		99	149		99		99	99	99	
GD5L								24		100	150		100		100	100	100	
GD6L								22		101	152		101		101	101	101	
GD7L								20		102	153		102		102	102	102	
GD8L								18		103	155		103		103	103	103	
GD9L								16		104	156		104		104	104	104	
GD10L								14		105	158		105		105	105	105	
GD11L								12		106	159		106		106	106	106	
GD12L								10		107	161		107		107	107	107	
GD13L								8		108	162		108		108	108	108	
GD14L								6		109	164		109		109	109	109	
GD15L								4		110	165		110		110	110	110	
GA1L										77	115		77		77	77	77	
GA2L										78	117		78		78	78	78	
GA3L										79	118		79		79	79	79	
GA4L										80	120		80		80	80	80	
GA5L										81	121		81		81	81	81	
GA6L										82	123		82		82	82	82	
GA7L										83	124		83		83	83	83	
GA8L										84	126		84		84	84	84	
GA9L										85	127		85		85	85	85	
GA10L										86	129		86		86	86	86	
GA11L										87	131		87		87	87	87	
GA12L										88	132		88		88	88	88	
GA13L										89	134		89		89	89	89	
GA14L										90	135		90		90	90	90	
GA15L										91	137		91		91	91	91	
GA16L										92	138		92		92	92	92	
GDSL										74	111		74		74	74	74	
GR/GWL										73	110		73		73	73	73	
MRFFTL											106						71	
MGFFTL											109						72	
MRDF2L											100		71					
MGDF2L											103		72					
MRDF1L											94		69					
MGDF1L										71	97		70					
MR68L										72	88							
MG68L											91							
MRFPPL											82				69			
MGFPPL											85				70			
RFDL								36			112							
DAVL								38			139							
B2GDSL								40			142							
MRGPL											76					69		
MGGPL											79					70		

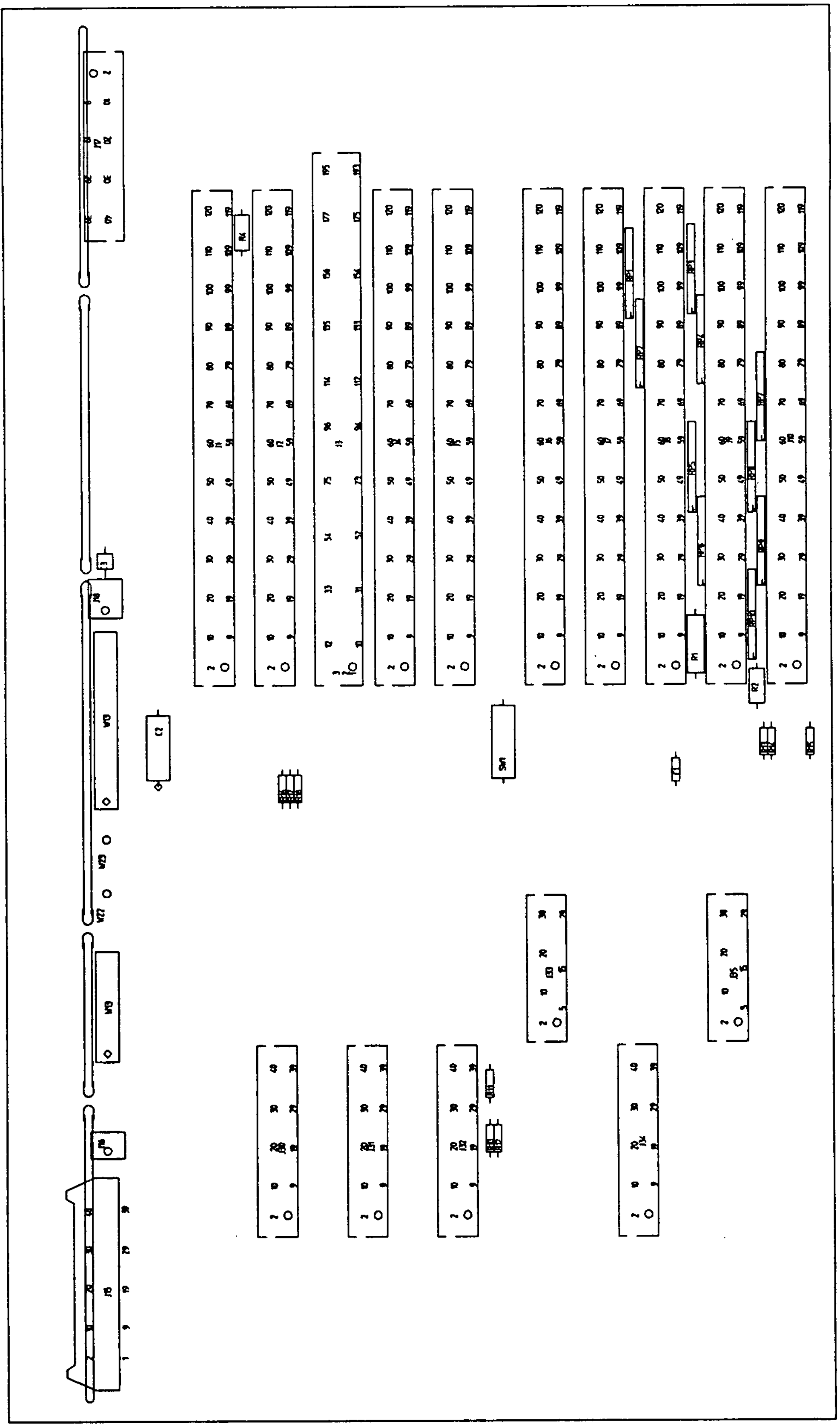


Figure 8-9. Motherboard Component Locator

A15
Keyboard

A15 Keyboard

The information in this section should be used to isolate faulty subblocks in the A15 Keyboard assembly. All procedures assume that you have used the Fault Isolation procedures in Section VII to determine this board has failed, and that you understand the Circuit Descriptions in Section VI.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Caution Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	Start troubleshooting by using figure 8-10. This procedure diagram describes the best order to perform the troubleshooting tests based on the symptoms observed.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
After-Repair	Use table 8-36 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. Several tests on the keyboard can be done from the front panel to isolate a failure.
2. Only +5 Vdc and ground are required to troubleshoot the A15 Keyboard assembly.
3. Disconnecting W10 from the A14 Mother Board puts the keyboard in a self-test mode.
4. If the name of a nonnumerical key or "Numbers Not Allowed" appears in the lower left of the display immediately after the power-up routine, there may be a stuck key or shorted trace on the keyboard. Start troubleshooting with the LEDs Test.
5. If the instrument does not respond to any key presses, there may be a stuck key. Start troubleshooting with the keyboard matrix subblock.

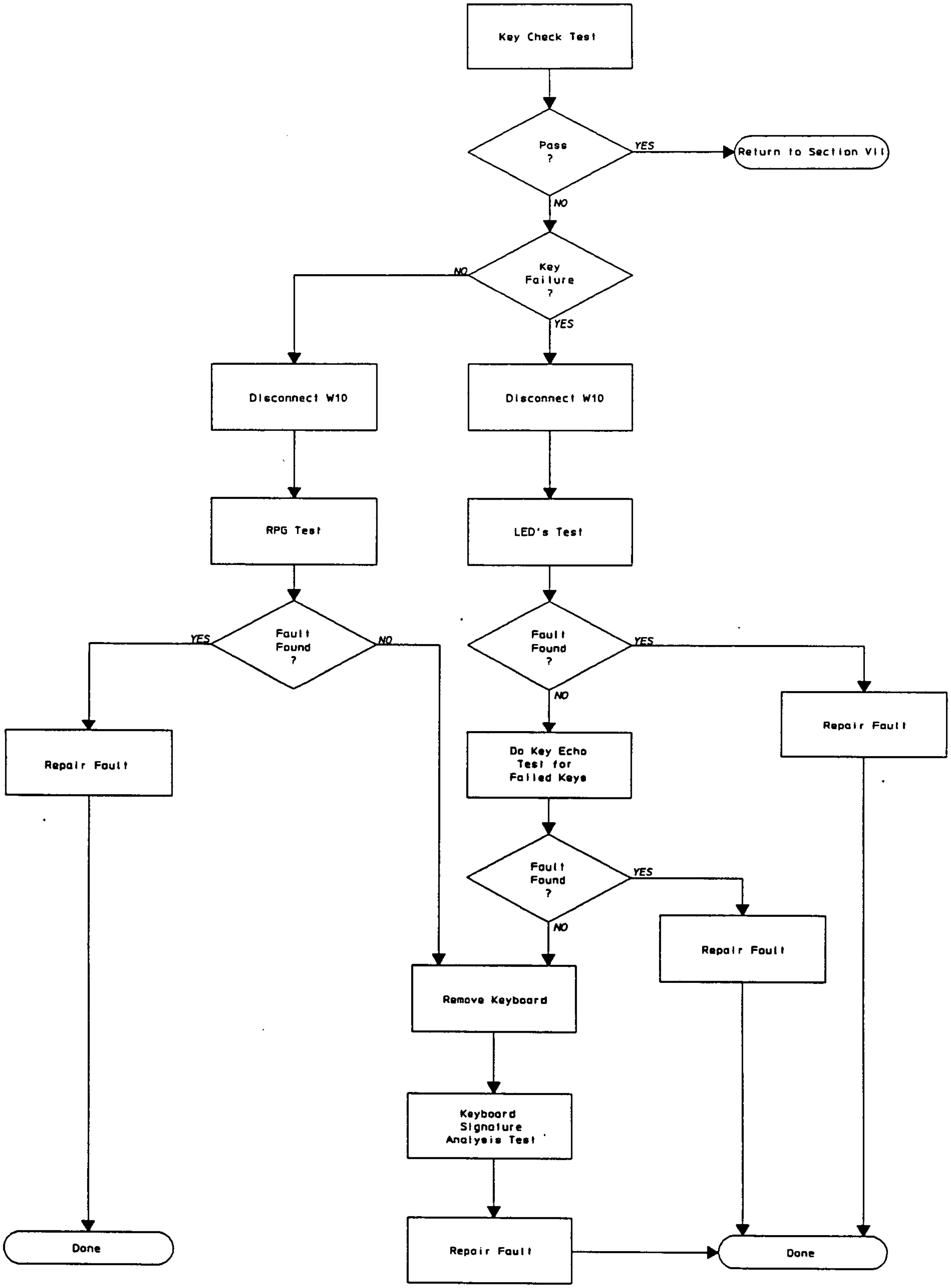


Figure 8-10. Keyboard Troubleshooting Procedure

Key Check Test

This test is done from the front panel before removing the keyboard.

1. Press the HP 3563A keys as follows:

   [Control]
   PRESET ...... RESET

2. Press every key on the keyboard except the Entry group keys (numbers, punctuation marks, **MARKER VALUE**, **BACK SPACE** and arrow keys) and the softkeys. The correct name of the key pressed should appear in the bottom left corner of the display.
3. Press **AVG** and then press all the keys in the ENTRY group except **MARKER VALUE**, **BACK SPACE** and the arrow keys. The correct name of the key pressed should appear in the bottom left corner of the display.
4. Press **SOURCE** and then press all the softkeys. The correct name of the softkey pressed should appear in the bottom left hand corner of the display.
5. Press **AVG** and rotate the Entry RPG. The numbers in the bottom left of the display should change as the RPG is turned.
6. Press **X** and rotate the Marker RPG. The numbers in the top left of the display should change as the RPG is turned.
7. If test fails, disconnect W10 (procedure follows) and proceed with the LEDs self-test.
8. If test passes, the keyboard is working correctly, return to Section VII,"Fault Isolation."

Disconnecting W10

1. Turn the HP 3563A OFF.
2. Disconnect the line power cable.
3. Remove the bottom cover.

Warning

230 Vdc may be present in the main A18 Power Supply board even with the line switch in the off position and the power cord removed. Be extremely careful when working in the proximity of this area. This high voltage could cause serious personal injury if contacted.

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4. Disconnect W10 from A14 J15.

Key Echo Test

This is a standalone self-test. Only +5V and ground are required. This test can be done from the front panel or with the keyboard removed. After the LEDs Test the keyboard automatically enters the key echo mode. In the Key Echo Test, the keyboard processor determines the key code of the key pressed. It then turns on LEDs corresponding to the key code.

1. Place all jumpers in the normal (N) position.
2. Disconnect W10 from the A14 Mother Board.
3. Connect the power cable and press the line switch ON.
4. Reset the keyboard by putting A15 J9 to the test (T) position, then back to the normal (N) position.
5. When the LEDs Test is finished (all the lights remain on), press the keys one at a time. As a key is pressed, its key code should be echoed along the bottom row of LEDs. Refer to table 8-30 for front panel location of LEDs. The key code for each key is listed in table 8-31.

Note

The only lights that should remain off after a key is pressed are the ones listed in table 8-31.

Table 8-30. LEDs Front Panel Location

Measuring	Ext Sample	A	B	Source	Ext Trigger	Channel 1 Over Range	Channel 2 Over Range
CR8	CR9	CR10	CR11	CR14	CR15	CR16	CR18

LEDs Test

This is a standalone self-test. Only +5V and ground are required. This test can be done from the front panel or with the keyboard removed. In the LEDs Test, the keyboard processor flashes the LEDs by using the data output register.

1. Disconnect the power cable.
2. Place all jumpers in the normal (N) position.
3. Disconnect W10 from from the A14 Mother Board.
4. Connect the power cable and press the line switch ON.
5. Reset the keyboard by putting A15 J9 to the test(T) position, then back to the normal (N) position.
6. To pass this test, the keyboard should respond as follows:
   a. Beep the beeper and flash all the LEDs three except CR12, CR17, and CR19. These LEDs will flash on and stay on since they are controlled by other boards.
   b. Beep the beeper and then light the LEDs one at a time in a pattern from left to right, top to bottom.
   c. Beep the beeper again and turn all the lights ON.
7. If only one or a few of the LEDs fail to flash, start troubleshooting with the LEDs subblock.
8. If all the LEDs fail to flash, proceed with the Key Echo Test (procedure follows).
9. If test passes, the following subblocks are most likely good:
   - Data Output Register
   - Keyboard Bus
   - LEDs
   - Upper half of Device Decoder
   - EPROM Decoder
10. Go to the Key Echo Test.

Table 8-31. Key Codes

KEY	LEDs Representing Key Codes Blank means light is off, X means light is on.							
	Measuring	Ext Sample	A	B	Source	Ext Trigger	Channel 1 Over Range	Channel 2 Over Range
	CR8	CR9	CR10	CR11	CR14	CR15	CR16	CR18
ARM			X	X	X	X		X
A			X	X	X			
B			X	X	X			X
A&B			X	X	X		X	
MEAS DISP			X	X	X	X		
VIEW INPUT			X	X	X		X	
STATE/TRACE		X						
SINGLE			X	X	X	X	X	
UPPER LOWER			X	X	X	X	X	X
FRONT BACK		X					X	
COORD			X	X	X		X	X
SCALE		X					X	X
UNITS		X						X
X				X	X	X	X	
Y				X	X			
XOFF				X	X	X		X
YOFF				X	X	X	X	X
SPCL MARKER					X	X		X
7			X				X	
8			X					
9			X					X
4			X		X		X	
5			X		X			
6			X		X			X
1			X		X	X		X
2			X		X	X	X	X
3			X		X	X	X	
0			X	X		X		X
.			X	X		X	X	X
,			X	X		X	X	
MARKER VALUE			X	X				
BACK SPACE			X	X			X	
—			X	X				X
START				X				
PAUSE CONT				X		X	X	
AUTO SEQ				X		X		X
MATH				X			X	X

Key Codes continued

KEY	LEDs Representing Key Codes Blank means light is off, X means light is on.							
	Measuring	Ext Sample	A	B	Source	Ext Trigger	Channel 1 Over Range	Channel 2 Over Range
	CR8	CR9	CR10	CR11	CR14	CR15	CR16	CR18
AUTO MATH				X	X		X	X
SAVE RECALL				X		X	X	X
SPCL FCTN				X				X
PRESET				X			X	
SYNTH				X		X		
CURVE FIT				X	X	X		
MEAS MODE					X	X	X	X
SELECT MEAS					X			X
WINDOW					X		X	
HELP				X	X		X	
AVG					X			
FREQ					X	X	X	
SOURCE					X	X		X
RANGE						X	X	X
INPUT COUPLE								X
SELECTTRIG						X		X
DISC						X		
PLOT					X	X		
ENGR UNITS								
CAL						X	X	
TRIG DELAY1							X	
HP-IB FCTN							X	X
LOCAL					X		X	X
↑		X				X		
↓		X				X		X
SOFTKEYS:								
SW 1			X			X	X	
SW 2			X			X		X
SW 3			X			X	X	X
SW 4			X				X	X
SW 5			X			X		
SW 6			X		X	X		
SW 7			X		X		X	X
SW 8			X	X			X	X

6. If only some of the key codes are incorrect, start troubleshooting with the keyboard matrix subblock.
7. If all key codes are incorrect or the LEDs do not light, remove the keyboard (refer to "Removing the Keyboard" procedure which follows) and then proceed with the signature analysis tests.
8. If this test passes, the keyboard matrix, keyboard processor, and LED's subblocks are rating correctly. Start troubleshooting with the command register and the handshake/interrupt subblocks.

RPG Test

The RPG Test is a standalone self-test requiring only +5 Vdc and ground. This test is done from the front panel before removing the keyboard. After the LEDs Test the keyboard automatically enters the key echo mode making this test possible. In the RPG Test, the keyboard processor determines which direction an RPG has turned and then flashes CR4, CR5, CR6, and CR7 in a pattern matching the direction the RPG turns.

1. Place all jumpers in the normal (N) position.
2. Disconnect W10 from the A14 Mother Board.
3. Connect the power cable and press the line switch ON.
4. Reset the keyboard by putting A15 J9 to the test (T) position, then back to the normal (N) position.
5. Note if CR1 (X), CR2 (Y), and CR3 (Enabled) flash three times and finally turn on and stay on.
6. If CR1, CR2, and CR3 do not operate correctly, start troubleshooting with the LEDs subblock.
7. Turn the Markers group RPG. Observe CR4(Remote), CR5 (Listen), CR6(Talk), and CR7 (SRQ). The LEDs should light in the same direction as the RPG is turned.
8. If CR4, CR5, CR6, and CR7 do not operate correctly, start troubleshooting with the RPG circuit subblock.
9. Repeat steps 7 and 8 except turn the Entry group RPG.
10. If the test passes, the RPG circuit subblock and corresponding keyboard processor lines are most likely working correctly. Remove the keyboard (see "Removing the Keyboard" procedure which follows) and then proceed with the signature analysis test.

Removing the Keyboard

Before removing the keyboard, disconnect W10 and run the LEDs Test, the Key Echo Test, and the RPG Test to determine the most likely failure.

1. Turn the line switch OFF.
2. Disconnect the power cord.
3. Remove the bottom cover.

Warning **230 Vdc may be present in the main A18 Power Supply board even with the line switch in the off position and the power cord removed. Be extremely careful when working in the proximity of this area. This high voltage could cause serious personal injury if contacted.**

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4. Disconnect W10 from A14 J15 and W17 from A14 J16.
5. Remove the four screws in the bottom of the front panel casting.
6. Remove top cover.
7. Disconnect the following cables:

Board	Cable	Connector
A33 Input	W1	A33 J300
A35 Input	W1	A35 J300
A31 Trigger	W5	A31 J1
A30 Source	W4	A30 J200

8. Remove the screws on the top and the sides of the front panel casting.
9. Remove the digital display's shield and the two screws on top of the digital display.
10. Remove wires x out, y out, and z out, which are on top of the digital display.
11. Pull out the digital display about one inch (2.54 cm).
12. The front panel can now be pulled away from the instrument's frame.
13. Disconnect RPG 1 from A15 J3 and RPG 2 from A15 J6.
14. Remove the 12 screws holding the keyboard to the front panel.
15. Connect +5 Vdc and ground to W17.

Keyboard Signature Analysis Tests

These tests are used when the previous tests fail to find the problem.

1. Disconnect power cable.
2. Put the test jumpers A15 J4, A15 J5, A15 J7, in the test(T) position.
3. Disconnect W10 from the A14 Mother Board.
4. Connect the signature analyzer according to table 8-32.

Table 8-32. Keyboad Signature Analyzer Setup

Signal	Polarity	Connection
Ground	—	A15 J1-1
Clock	Negative Edge	A15 J1-3
Stop	Positive Edge	A15 J1-4
Start	Positive Edge	A15 J1-5

5. Connect the power cable and press the line switch ON.

Table 8-33. Keyboard Signature Analysis Test ONE

Jumpers in test (T) position J4. J5. J7
Jumpers in normal (N) position: J2. J8. J9
Signature Analyzer Setup. Refer to table 8-32
+5 V Signature = 980H

Component	Pin	Signature	Component	Pin	Signature
U106	2	P75C	U206	15	3799
	3	H843		16	2U06
	4	38A3		17	15UO
	5	5PUU		18	3443
	6	5H3U		19	9FA6
	7	9U1H		21	HFU1
	8	H182		22	H182
	9	HFU1		23	9U1H
				24	5H3U
				25	5PUU
				26	38A3
				27	H843
				28	P75C

Table 8-34. Keyboard Signature Analysis Test TWO

Jumpers in test (T) position: J2. J4. J5. J7
Jumpers in normal (N) position: J8. J9
Signature Analyzer Setup: Refer to table 8-32
+5 V Signature = 980H

Component	Pin	Signature	Component	Pin	Signature
U108	2	980H	U302	9	980H
	3	0000		8	0000
	4	0000		7	980H
	5	980H		6	980H
	6	980H		5	980H
	7	980H		4	0000
	8	0000		3	0000
	9	980H		2	980H
	12	P75C	U308	7	3565
	13	H843		9	02UF
	14	38A3		10	1A63
	15	5PUU			
	16	5H3U			
	17	9U1H			
	18	H182			
	19	HFU1			
U208	9	9C08			
	10	0U33			
	11	P1AU			
	13	5PFC			
	14	11U0			
	15	C529			
	16	189F			
	17	9HC9			

Table 8-35. Keyboard Signature Analysis Test THREE

Jumpers in test (T) position: J2. J4. J5. J7
Jumpers in normal (N) position: J8. J9
Signature Analyzer Setup: Refer to table 8-32
+5 V Signature = 980H

Component	Pin	Signature
U308	12	3565
	13	02UF
	14	1A63
	15	C5U7

Keyboard After-Repair Adjustments and Tests

Table 8-36. After-Repair Adjustments and Tests

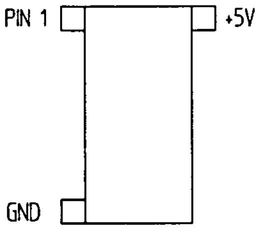
Perform the following:*	Section
Key Check Test (A)	VIII
Diagnostic Tests: Test All	VII
Adjustments: None	—
Operational Verification: None	—
Performance Tests: None	—

*Return all jumpers to the normal (N) position

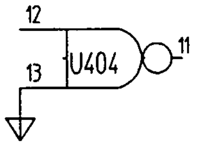
REFERENCE TABLE

IC	GND	+5V	CAPS
U105	7	14	C105
U106	1,10	20	C106
U108	10	20	C108
U210	7	14	C210
U205	7	14	C205
U206	20	40	C206
U208	12 18,20	21,24	C208
U300	1,10	20	C300
U301	1 19,10	20	C301
U302	10	20	C302
U303	1 19,10	20	C303
U304	1,10	20	C304
U305	1,10	20	C305
U306	7,8	16	C306
U307	8	16	C307
U308	8	16	C308
U402	7	14	C402
U404	7	14	C404

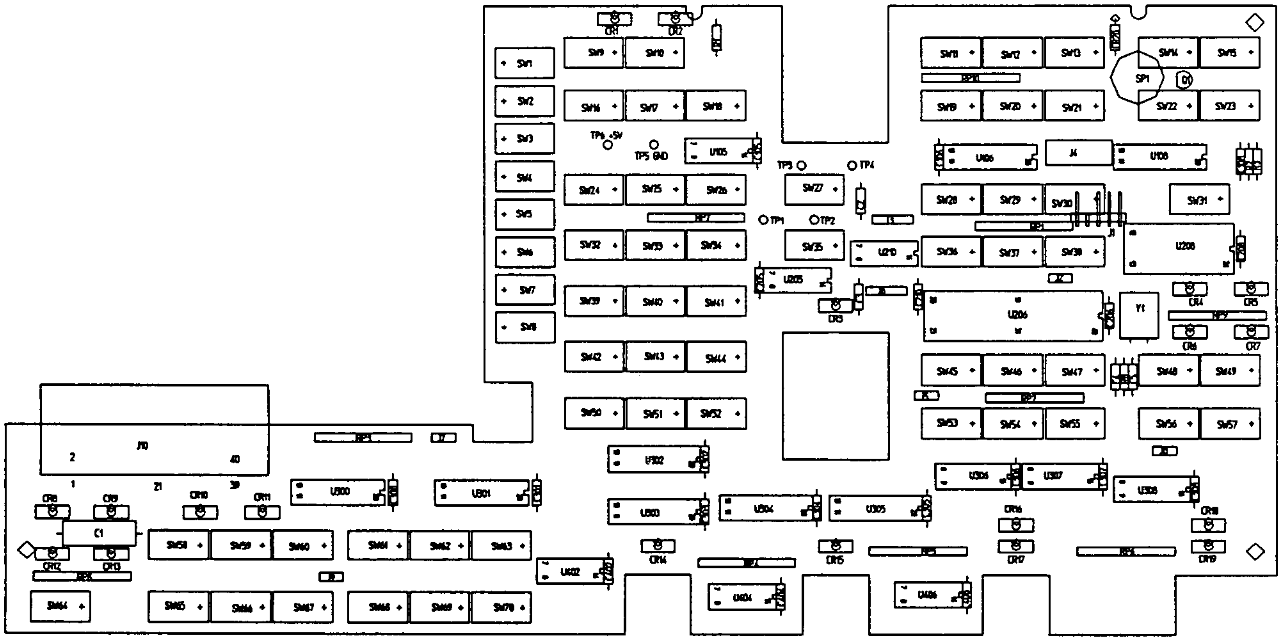
ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED TO PIN 8 AND +5 V IS CONNECTED TO PIN 16).



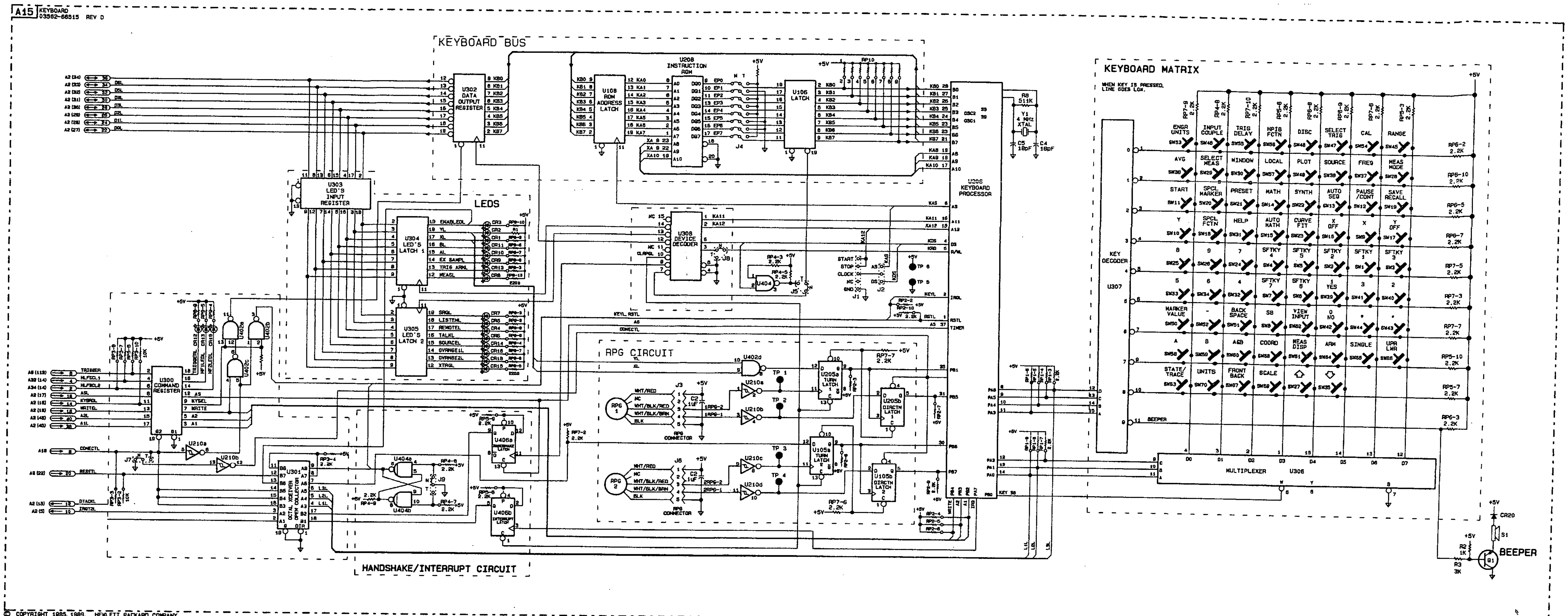
NOT
USED



A15 Keyboard Ground and Power
P/N 03562-66515 Rev D



A15 Keyboard Component Locator
P/N 03562-66515 Rev D
Page 2 of 3



A15 Keyboard Schematic
P/N 03562-66515
Page 3 of 3

A18
Power Supply

A18 Power Supply Assembly

The information in this section should be used to isolate faulty subblocks in the A18 power supply assembly. All procedures assume that you have used the Fault Isolation procedures in Section VII to determine this board has failed, and that you understand the Circuit Descriptions in Section VI.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by Insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	Start troubleshooting by using figure 8-11. This procedure diagram describes the best order to perform the troubleshooting tests based on the symptoms observed.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
Verify	Use table 8-37 to verify the power supply is operating correctly. Use the oscilloscope waveforms in table 8-38 to see correct operation at various test points in the assembly.
After-Repair	Use table 8-39 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. The power supply must have a load to operate. Putting jumper A18 J100 in the test position provides a load for the +5V supply. The secondary connectors W11 (rear of display unit), W13 (A18 J1), W16(A18 J400), W22, and W23 can be disconnected and the power supply serviced independently of the other boards.
2. If the power supply intermittently powers down or fails to turn on, check the powerdown circuit. A18 R1 may be out of adjustment. Refer to Section III for the adjustment procedure.
3. If the instrument cold starts but then fails to turn on when power is cycled later, the most likely cause is the pulse width modulator (U101).

Table 8-37. Power Supply Nominal Values
Return Location is A18 TP13

Supply Name	Output Location	Nominal Voltage	Voltage Tolerance	Ripple Tolerance
+30V	A18 J1-1	+30V	± 1.8V	10 mV
– 30V	A18 J1-2	– 30V	± 1.8V	10 mV
+15A	A18 J1-3	+15V	± 0.9V	10 mV
– 15A	A18 J1-4	– 15V	± 0.9V	10 mV
+5S	A18 J1-5	+5V*	± 0.3V	50 mV
+2.6V	A18 J1-6	+2.6V	± 0.16V	50 mV
+8S1	A18 J1-7	+8V	± 0.48V	25 mV
+8S2	A18 J1-8	+8V	± 0.48V	25 mV
+15S	A18 J1-9	+15V	± 0.9V	25 mV
– 15S	A18 J1-10	– 15V	± 0.9V	25 mV

*Note: If secondary connectors are disconnected and J100 is in test (T) position, the +5S supply equals +5.2 ± 0.1V.

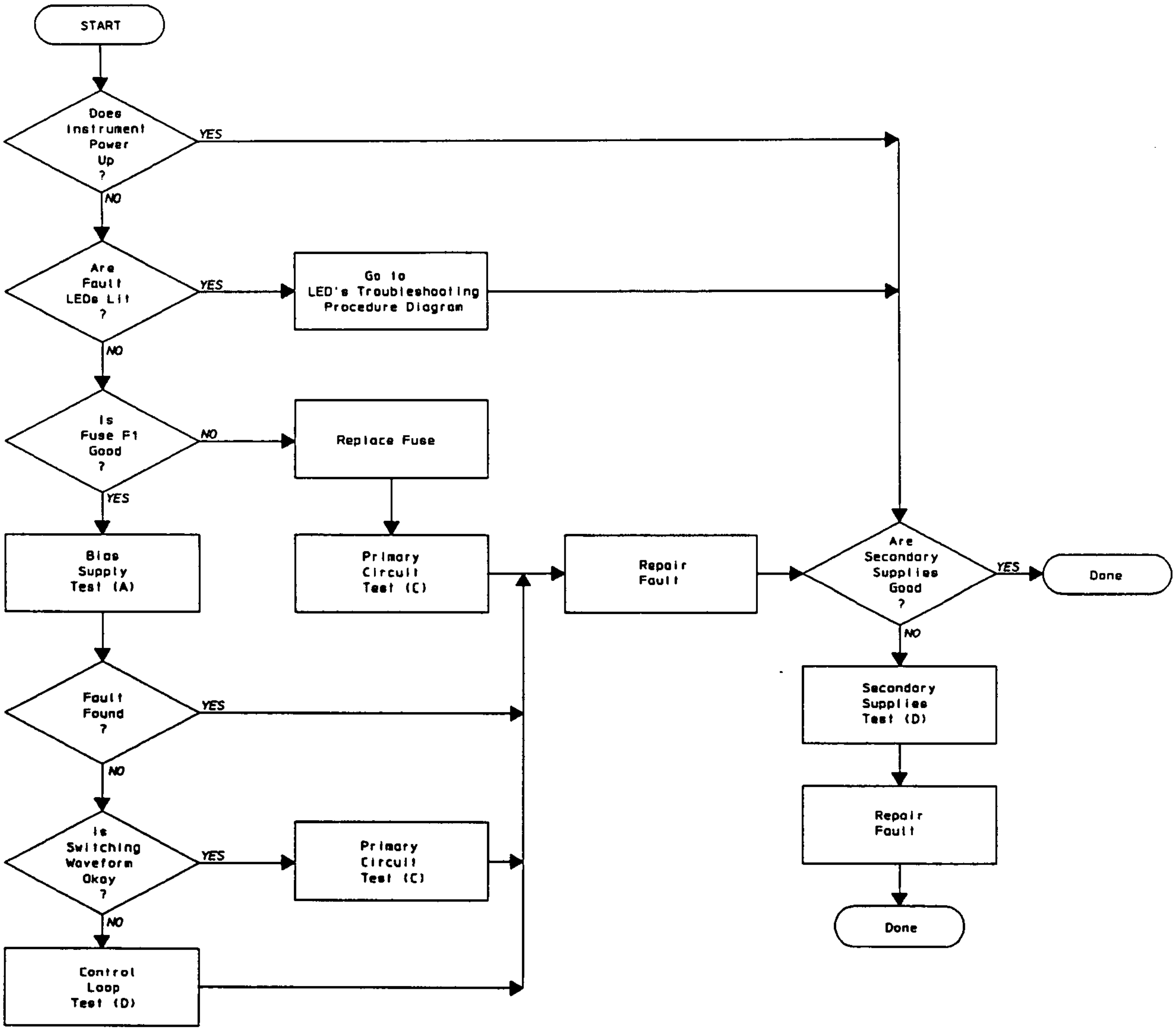


Figure 8-11. Power Supply Troubleshooting Procedure Diagram

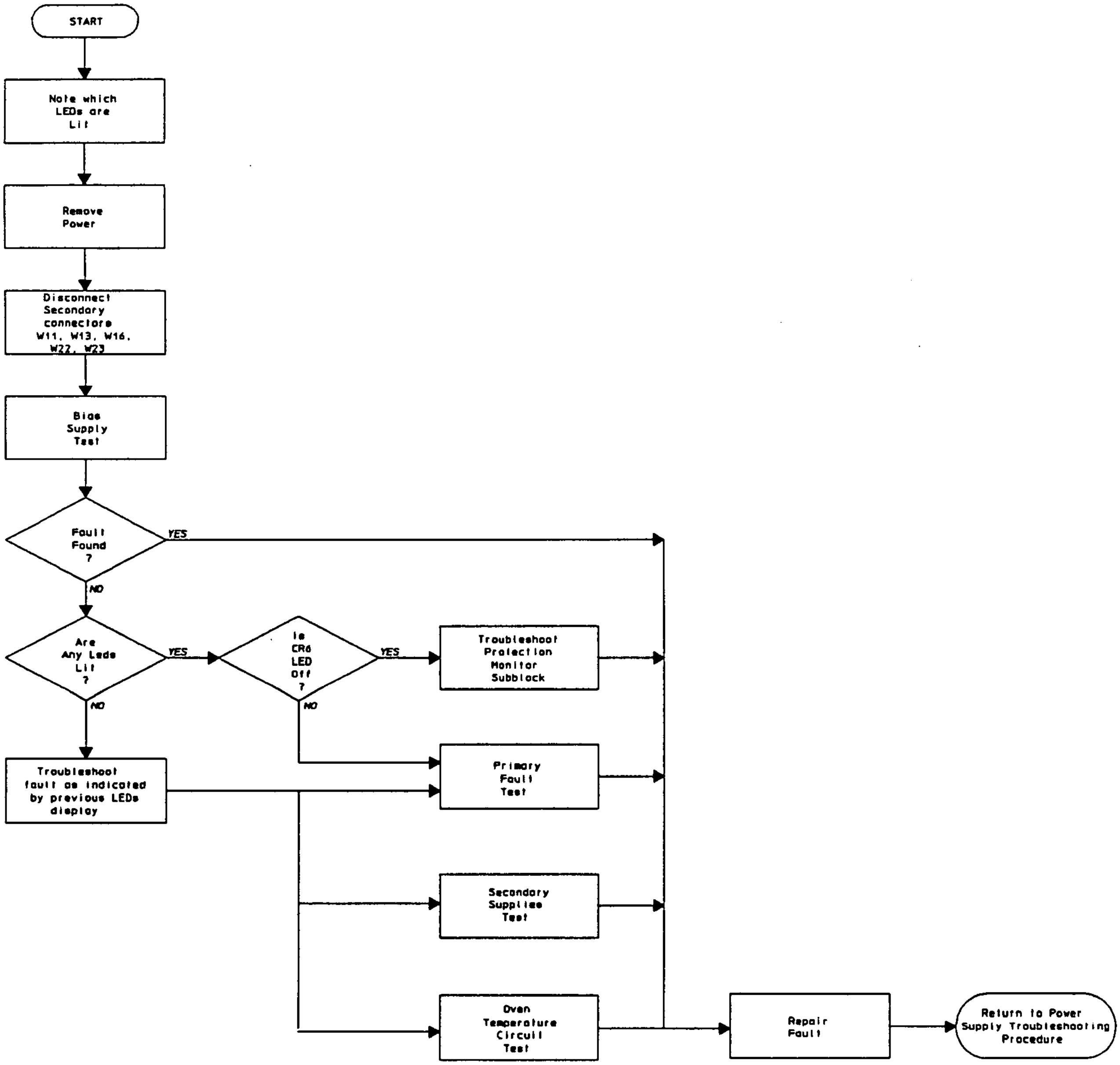

START
Note which LEDs are Lit
Remove Power
Disconnect Secondary connectors W11, W13, W16, W22, W23
Bias Supply Test
Fault Found ?
YES
NO
Are Any Leds Lit ?
YES
Is CR6 LED Off ?
YES
Troubleshoot Protection Monitor Subblock
NO
NO
Troubleshoot fault as indicated by previous LEDs display
Primary Fault Test
Secondary Supplies Test
Oven Temperature Circuit Test
Repair Fault
Return to Power Supply Troubleshooting Procedure

Figure 8-12. Fault LEDs Troubleshooting Procedure Diagram

Bias Supply Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning **Even with power removed, energies capable of personal injury are present in this circuit. With the jumpers in the TEST position, these voltages will discharge to relatively safe levels after approximately sixty seconds.**

---

2. Connect the power cable and press the line switch ON.
3. Connect the voltmeter negative terminal to the HP 3563A chassis.
4. Connect the voltmeter positive terminal to A18 TP11. The dc voltage should be +12 ± 0.72V.
5. Connect the voltmeter positive terminal to A18 TP10. The dc voltage should be − 12 ± 0.72V.
6. If this test fails, troubleshoot the bias supply subblock back to the line filter.
7. If the test passes, the bias supply subblock is all right. Return to the troubleshooting procedure diagrams.

Primary Fault Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning

Even with power removed, energies capable of personal injury are present in this circuit. With the jumpers in the TEST position, these voltages will discharge to relatively safe levels after approximately sixty seconds.

---

2. Using insulated, needle-nose pliers, set jumpers A18 J401, A18 J402, and A18 J100 to the test (T) position. It is not necessary for A18 J100 to have a jumper. Connect center pin and pin closest to the center of the instrument for the test (T) position.
3. Connect the voltmeter from the gate to drain of A18 Q400. Note resistance measurement.
4. Connect the voltmeter from the gate to drain of A18 Q401. Note resistance measurement.
5. If the resistance measurement of either FET is equal to or less than 20 k, replace the FET. Check the following resistors and replace any that are not the correct-value:

Resistor	Value
A18 R409	18 ± 1 Ω
A18 R410	3.9k ± 200 Ω
A18 R403	18 ± 1 Ω
A18 R404	3.9k ± 200 Ω

6. Set jumpers A18 J401 and A18 J402 to normal position and the rear panel voltage selector switch to 115V.

Caution

If the rear panel voltage selector switch is changed from the 220V position to the 115V position, it must be changed back after completing this test.

---

7. Connect the triple output supply to the bias supply subblock as follows:

   +15 Vdc to (+) side of A18 C107
   – 15 Vdc to (–) side of A18 C100
   +5 Vdc to A18 U2 pin 4
   Ground to A18 TP13

8. Check Waveform #4 at A18 TP5 and A18 TP6. If the waveforms are incorrect, go to the "Control Loop Test" procedure.
9. Connect the variable ac power supply to the power line connector. Set supply to 25 ± 2 Vac.
10. Check Waveforms #5, #6, and #8. If the waveforms are incorrect, troubleshoot the primary transformer and diode circuits.
11. If the Waveforms #5, #6, and #8 are all right, connect the voltmeter to the +5V regulator A18 U502 pin 1.
12. Slowly increase the variable ac power supply until A18 U502 regulates or the variable ac power supply reaches 129 Vrms.
13. If the voltmeter reading is greater than 5.3 Vdc or A18 U502 did not regulate, go to the "Control Loop Test".
14. If the voltmeter reading is 5 ± 0.3 Vdc, go to the "Slow Start Test".

Caution

If the rear panel voltage selector switch was changed from the 220V position to the 115V position, it must be changed back to the 220V position.

Primary Circuit Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning **Even with power removed, energies capable of personal injury are present in this circuit. With the jumpers in the TEST position, these voltages will discharge to relatively safe levels after approximately sixty seconds.**

---

2. Using insulated, needle-nose pliers, set jumpers A18 J401 and A18 J402 to the test(T) position.
3. Connect the voltmeter from the gate to drain of A18 Q400. Note resistance measurement.
4. Connect the voltmeter from the gate to drain of A18 Q401. Note resistance measurement.
5. If the resistance of either FET is equal to or less than 20 kΩ, replace the FET. Check the following resistors and replace any that are not the correct value:

Resistor	Value
A18 R409	18 ± 1 Ω
A18 R410	3.9k ± 200 Ω
A18 R403	18 ± 1 Ω
A18 R404	3.9k ± 200 Ω

6. Set jumpers A18 J401 and A18 J402 to normal position and the rear panel voltage selector switch to 115V.
7. Disconnect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), and W16 (A18 J400). Unscrew W22 and W23 from the A14 mother board.
8. Set jumper A18 J100 to the test (T) position.
9. Connect A18 TP13 (ground) to A18 TP2.
10. Connect the variable ac power supply to the power line connector.
11. Connect the voltmeter positive lead to the +Vdc side of A18 C406.

12. Connect the voltmeter negative lead to the – Vdc side of A18 C402.
13. Slowly increase the voltage of the variable ac power supply to 129 Vrms while monitoring the voltmeter reading.
14. If the voltmeter reading is 360 ± 20 Vdc when the variable ac power supply is 129 Vrms, the bulk supply is all right.
15. Disconnect A18 TP2 from A18 TP13. Disconnect the test instruments from the HP 3563A.
16. Connect secondary connectors W11 (rear of the display unit), W13 (A18 J1), W16(A18 J400), W22, and W23.
17. Set A18 J100 to the normal (N) position.
18. Return to the troubleshooting procedure diagrams.

Control Loop Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning **Even with power removed energies capable of personal injury are present in this circuit. With the jumpers in.the TEST position, these voltages will discharge to relatively safe levels after approximately sixty seconds.**

---

2. Using insulated, needle-nose pliers, set jumpers A18 J401 and A18 J402 to the test (T) position.
3. Disconnect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), and W16 (A18 J400). Unscrew W22 and W23 from the A14 mother board.
4. Put A18 J100 in the test (T) position.
5. Connect the dc power supply negative lead to W23 and the dc power supply positive lead to W22.
6. Connect the voltmeter negative terminal to the HP 3563A chassis and the positive terminal to A18 TP7.
7. Connect the power cord and press the line switch on.
8. Vary the dc power supply and monitor the control voltage at A18 TP7. When the dc supply is greater than 5.2V the control voltage should be 0.6 ± 0.05V. When the dc supply is less than 5.2V the control voltage should be 4.5 ± 0.4V.
9. If the control voltage does not respond correctly as the dc supply voltage is varied, troubleshoot the current monitor and error voltage subblocks.
10. Connect Channel 1 of the oscilloscope to A18 TP5 and Channel 2 to A18 TP6.
11. Vary the dc power supply and monitor the switching waveform (Waveform #4). When the dc supply is greater than 5.2V the switching waveform pulse width should be zero. When the dc supply voltage is less than 5.2V the switching waveform pulse width should be maximum (45% or 2.4 μs).
12. If the switching waveform does not respond correctly as the dc supply voltage is varied, troubleshoot the pulse width modulator and chopper isolation/driver subblocks.

13. Disconnect the power cord. Connect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), W16 (A18 J400), W22 and W23.
14. Put jumper A18 J100 in the normal position.
15. Return to the troubleshooting procedure diagrams.

Slow Start Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning **Even with power removed, energies capable of personal injury are present in this circuit. With the jumpers in the TEST position, these voltages will discharge to relatively safe levels after approximately sixty seconds.**

---

2. Using insulated, needle-nose pliers, set jumpers A18 J401 and A18 J402 to the test (T) position.
3. Using 10:1 scope probes, connect channel 1 to A18 TP5 and channel 2 to A18 TP6. Set the two channel oscilloscope as follows:

Mode	A & B
CH1 V/Div	500 mV/Div
CH2 V/Div	500 mV/Div
CH1 Coupling	dc
CH2 Coupling	dc
Time/Div	2.00 μs/Div
EXT Trigger	EXT + 1
—	A18 TP1

4. Refer to Waveform #4 (Power Supply Signal Waveforms section). Monitor the oscilloscope while cycling the power on the HP 3563A.
5. The switching waveforms duty cycle should increase from 0% to 45% in 0.1s. The control voltage at A18 TP7 should also go from 0V to 4.5 ± 0.4V in 0.2s.

Secondary Supplies Test

Caution

Do not attempt this test if the Over Temperature LED or the Primary Fault Fault LED is lit when the HP 3563A is turned on. Also verify that the Bias Supply is operating correctly. Grounding A18 TP9 defeats the protection monitor which may result in damage to the HP 3563A circuit boards.

---

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning

Even with power removed energies capable of personal injury are present in this circuit. These voltages will discharge to relatively safe levels after approximately one minute.

---

2. Jumpers A18 J401 and A18 J402 should be in the normal position.
3. Disconnect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), and W16 (A18 J400). Unscrew W22 and W23 from the A14 mother board.
4. Put jumper A18 J100 in test (T) position.
5. Connect the power cord and press the line switch ON.
6. Compare the output voltages to table 8-37. The +5S supply should be 5.2 ± 0.1 Vdc.
7. If all the voltages are within specification, perform the following:
   a. Ground A18 TP12 briefly to reset the HP 3563A.
   b. If any LEDs are lit, troubleshoot the comparators in the protection monitor subblock.
   c. If no LEDs are lit, troubleshoot the fault as indicated by the previous LED display.

8. If the voltages are not within specification, perform the following:

   a. Starting with the +5V supply check each secondary regulator (A18 U500 to A18 U508) to by measuring the following points:
      - Voltage at pin 1 should be 2.5V greater than voltage at pin 0.
      - Voltage at pin A should be 1.25V greater than voltage at pin 0.
      - Replace any faulty regulators.
      - If voltages are now in specification, go to step 9.

   b. Check the + 5V secondary Waveform #9 and the secondary supplies Waveform #10.

   c. If waveforms are all right, troubleshoot the secondary supplies back to the primary transformer. If problem is not found, go to the "Control Loop Test" procedure.

   d. If the waveforms are incorrect, troubleshoot back to the chopper switches starting with the secondary diodes A18 CR300, A18 CR301, A18 CR512 to A18 CR514, A18 CR600 to CR603.

9. Disconnect the power cord. Connect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), W16 (A18 J400), W22 and W23.

10. Put jumper A18 J100 in the normal position.

11. Return to troubleshooting procedure diagrams.

Over Temperature Circuit Test

1. Disconnect the power cord from the rear panel. Remove the bottom cover and the power supply shield of the HP 3563A.

Warning **Even with power removed, energies capable of personal injury are present in this circuit. These voltages will discharge to relatively safe levels after approximately one minute.**

---

2. Jumpers A18 J401 and A18 J402 should be in the normal position.
3. Allow 20 minutes for all components to cool off.
4. Disconnect secondary connectors W11 (rear of the display unit), W13 (A18 J1), W16 (A18 J400). Unscrew W22 and W23 from the A14 mother board.
5. Put A18 J100 in the test (T) position.
6. Connect power cord and press the line switch on.
7. If the OTEMP LED is not lit, the over temperature circuit is operating correctly. First check that the fan is operating. If the fan is operating, check each subblock of the power supply starting with the bias supply (see “Bias Supply Test”) until the fault is found.
8. If the OTEMP LED is lit, the over temperature circuit is faulty. Perform the following steps:
    a. Check the voltage of U104 pin 14. It should be +5 0.3 Vdc.

    b. If the voltage is correct, ground A18 TP12 briefly to reset the HP 3563A. If the LED is on, replace U100.

    c. Check the inputs of U104. At 25° centigrade pin 8 of U104 should equal 3 ± 0.2 Vdc and pin 9 of U104 should equal 3.5 ± 0.2 Vdc.

    d. Replace faulty part.

9. Disconnect the power cord.

Warning **Even with power removed, energies capable of personal injury are present in this circuit. These voltages will discharge to relatively safe levels after approximately one minute.**

---

10. Connect the secondary connectors W11 (rear of the display unit), W13 (A18 J1), W16 (A18 J400), W22 and W23.
11. Put jumper A18 J100 in the normal position.
12. Return to troubleshooting procedure diagrams.

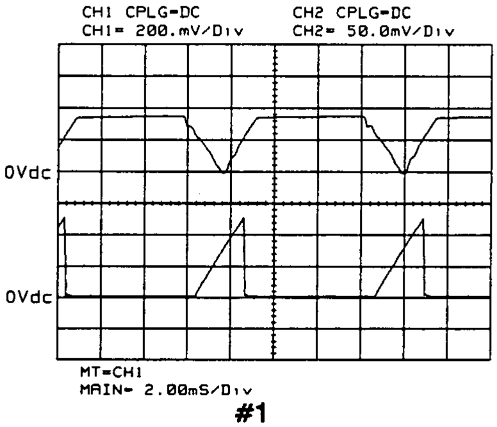
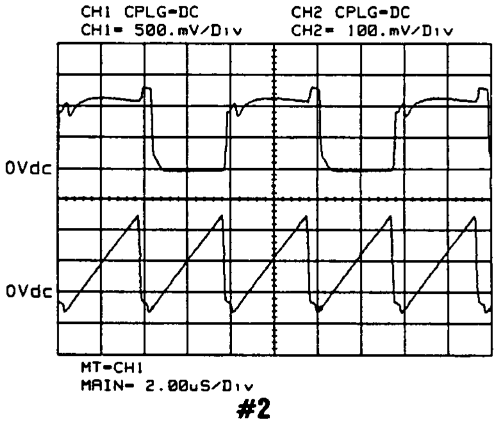
Power Supply Signal Waveforms

The oscilloscope plots are used for troubleshooting the A18 Power Supply. Note that all the measurements are taken with a **10:1** probe. Other notes unique to a measurement are written next to the waveform.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock.**

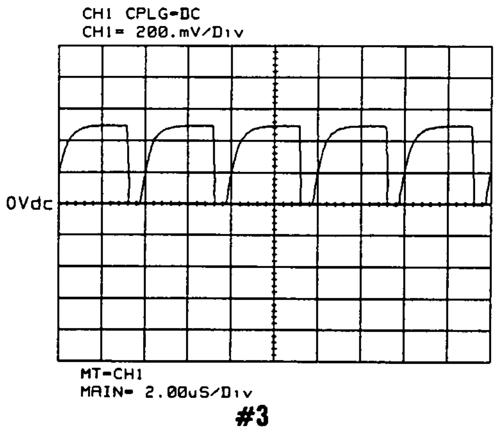
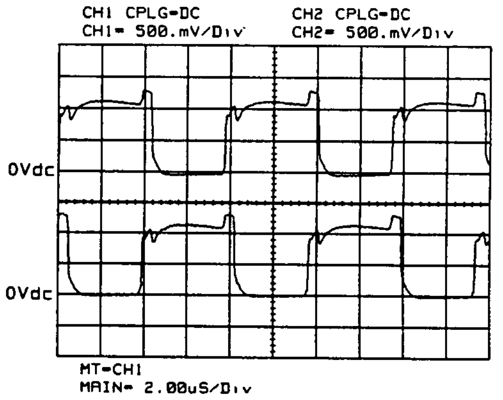
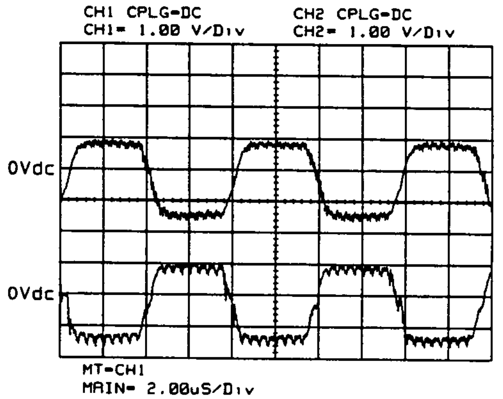
Table 8-38. Power Supply Signal Waveforms

Remove power
Jumpers in test position: A18 J401 A18 J402
Connect ground to A18 TP13
Probe type 10:1
Power ON

Setup	Parameters	Waveforms
U2 Connect CH1 to A18 U2 pin 4 Connect CH2 to A18 U2 pin 6 Oscilloscope: Mode A & B CH1 V/Div 200 mV/Div CH2 V/Div 50 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 ms/Div Trigger CH1	Pulse shape Amplitude Time Relationship	 #1
Driver and PWM Clock Connect CH1 to A18 TP5 Connect CH2 to A18 TP1 Oscilloscope: Mode A & B CH1 V/Div 500 mV/Div CH2 V/Div 100 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 µs/Div Trigger CH1	Pulse shape Duty cycle Time Relationship The triangle wave must start at 0± 0.200 Vdc	 #2

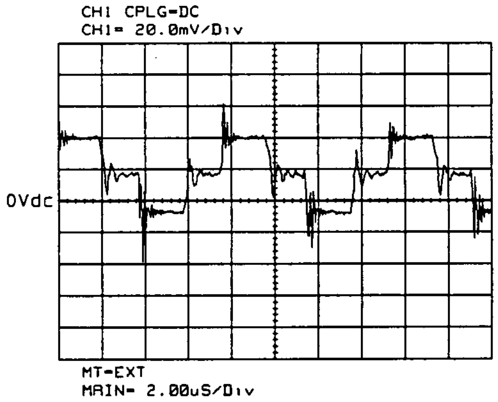
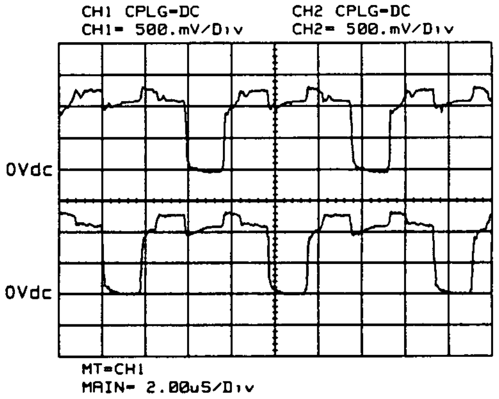
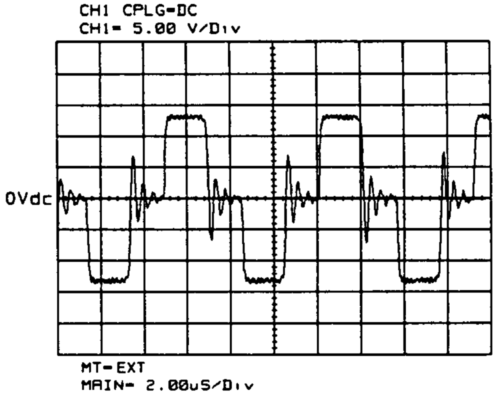
Power Supply Signal Waveforms continued

Remove power
Jumpers in test position: A18 J401 A18 J402
Connect ground to A18 TP13
Probe type 10:1
Power ON

Setup	Parameters	Waveform
SYNC Connect CH1 to A18 TP3 Oscilloscope: Mode A CH1 V/Div 200 mV/Div CH1 Coupling dc Time/Div 2 μs/Div Trigger CH1	Pulse shape Duty cycle	 #3
Test Switching Waveform Connect CH1 to A18 TP5 Connect CH2 to A18 TP6 Oscilloscope: Mode A & B CH1 V/Div 500 mV/Div CH2 V/Div 500 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 μs/Div Trigger CH1	Pulse shape Time Relationship	 #4
Power FET Gates Connect CH1 to the gate of A18 Q401 Connect CH2 to the gate of A18 Q400 Oscilloscope: Mode A & B CH1 V/Div 1 V/Div CH2 V/Div 1 V/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 μs/Div Trigger CH1	Pulse shape Time Relationship **Note: Signals will be noisy**	 #5

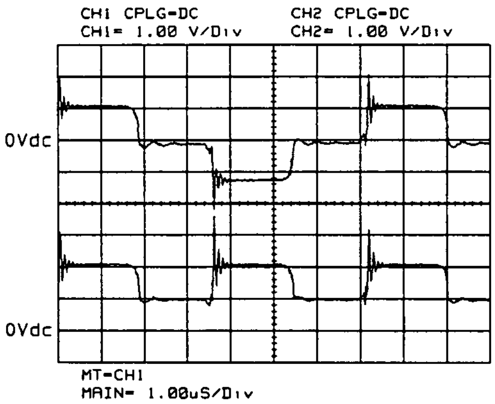
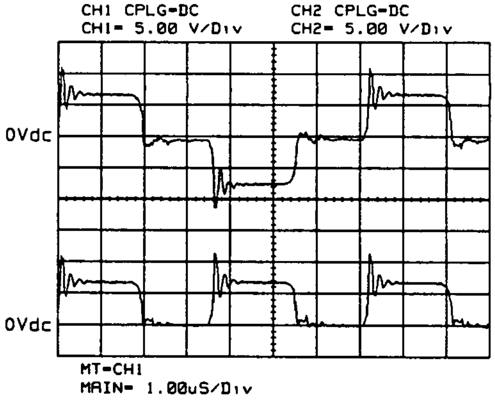
Power Supply Signal Waveforms continued

Remove power
Jumpers in test position. All jumpers in normal position
Connect ground to A18 R800
Probe type 10:1
Power ON

Setup	Parameters	Waveform
Transformer T2 (Primary Current) Connect CH1 to A18 TP8 Oscilloscope: Mode A CH1 V/Div 20 mV/Div CH1 Coupling dc Time/Div 2 μs/Div Trigger EXT 1,A18TP1	Pulse shape Duty cycle	 **#6**
Normal Switching Waveforms Connect CH1 to A18 TP5 Connect CH2 to A18 TP6 Oscilloscope: Mode A & B CH1 V/Div 500 mV/Div CH2 V/Div 500 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 μs/Div Trigger CH1	Pulse shape Only one signal on at a time (0V)	 **#7**
FA - FB (T1, primary voltage) Connect CH1 to FA of A18 T1 Connect CH2 to FB of A18 T1 (across primary transformer) Oscilloscope: Mode A & B CH1 V/Div 5 V/Div CH2 V/Div 5 V/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 μs/Div Trigger CH1	Pulse shape Duty cycle	 **#8**

Power Supply Signal Waveforms continued

Remove Power
Jumpers in test position: All jumpers in normal position
Connect ground to A18 TP13
Probe: 10:1
Power On

Setup	Parameters	Waveform
+5V Secondary Connect CH1 to A18 CR300 Anode Connect CH2 to A18 CR300 Cathode Oscilloscope: Mode A & B CH1 V/Div 1 V/Div CH2 V/Div 1 V/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH1	Pulse shape	 #9
Secondary Supplies Connect CH1 to A18 CR601 Anode Connect CH2 to A18 CR601 Cathode Oscilloscope: Mode A & B CH1 V/Div 5 V/Div CH2 V/Div 5 V/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH1	Pulse shape	 #10

Power Supply After-Repair Adjustments and Tests

Table 8-39. After-Repair Adjustments and Tests

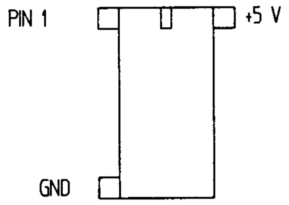
Perform the following:*	Section
Diagnostic Tests: TESTALL	VII
Adjustments: Do the power-down adjustment only if a component was changed in the power-down or bias supply subblocks.	III
Operational Verification: None	—
Performance Tests: None	—

*Return all jumpers to the normal (N) position

REFERENCE TABLE

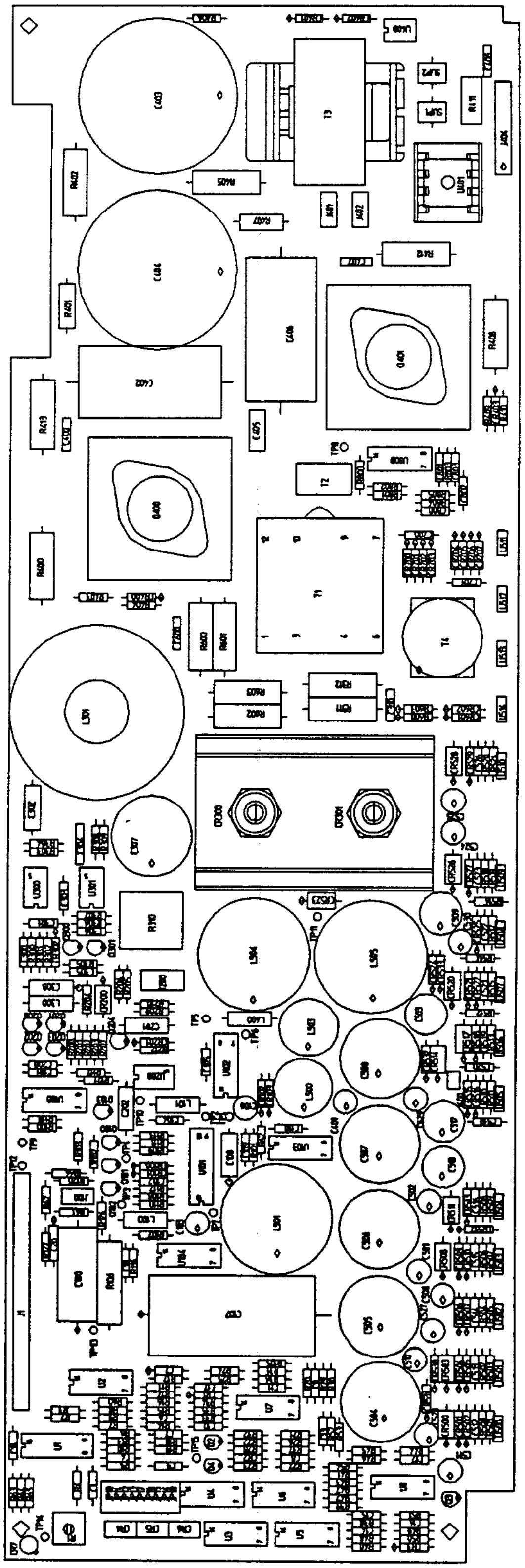
IC	GND	+5VB	CAPS	-12B	+12B
U1	8	15,16			
U2	12				3
U7	12				3
U8	12				3
U100	7	14	C101		
U101	6,7 15,11				17
U102	7				
U103	7	14	C110		
U104	12				3
U200				4	7
U300				4(C300)	7(C306)
U301				4	7
U800	3,8	11	C803	6(C802)	

ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED TO PIN 8 AND +5 V IS CONNECTED TO PIN 16).

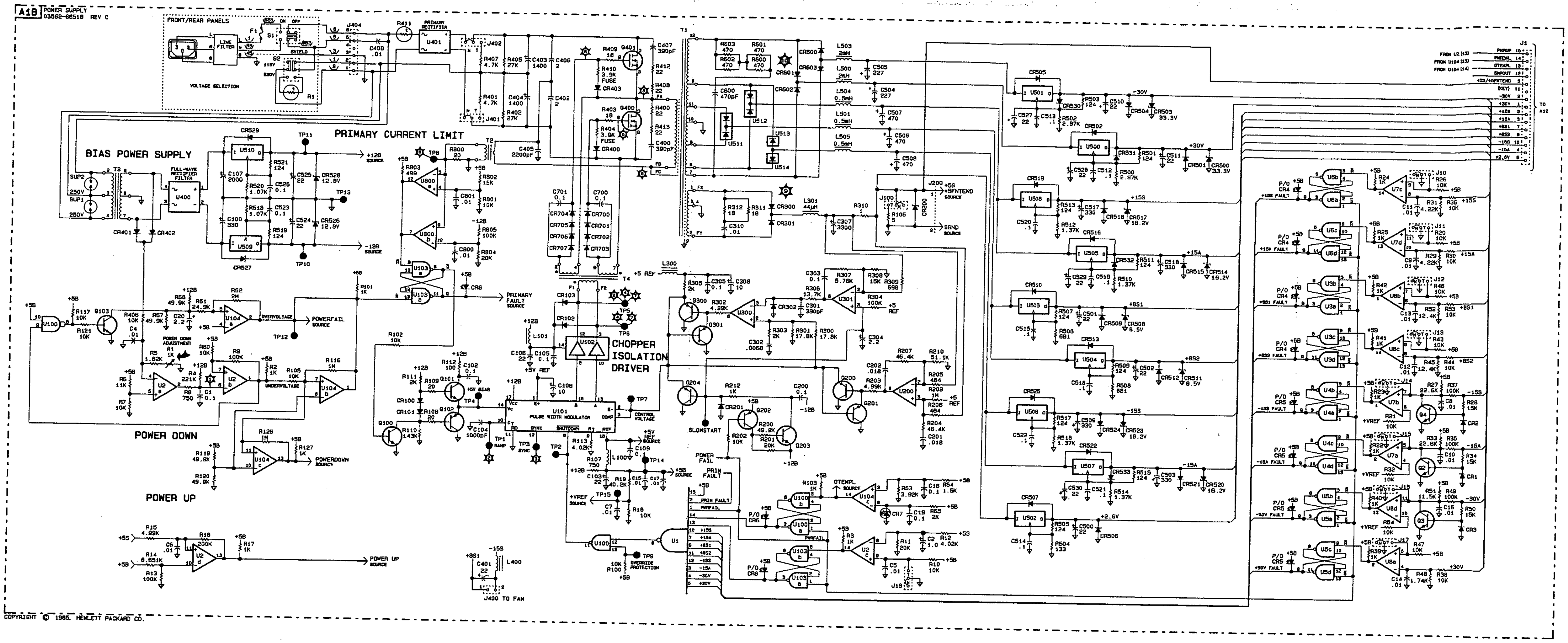


A18 Power Supply Ground and Power Chart

P/N 03562-66518 Rev C



A18 Power Supply Component Locator
P/N 03562-66518 Rev C



A18 Power Supply Schematic
P/N 03562-66518
Page 3 of 3

A30
Analog Source

A30 Analog Source

The information in this section should be used to isolate faulty subblocks on the analog source board. All procedures assume that you have used the fault isolation procedures in Section VII to determine that this board has failed and that you have read and understand the circuit descriptions in Section VI.

Warning

Service procedures described in this section are performed with protective covers removed and power applied. Hazardous voltages in these circuits can cause personal injury if you make an electrical connection between you and them. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A while power is on. Power transients caused by insertion or removal may cause damage to circuits on the board being changed or on other boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start The main circuits on this board are the sine wave circuitry (across the top of the schematic), the offset circuits (includes the front end interface), the calibrator (and its two signal sources), and the overload detection circuit. Choose the circuit to troubleshoot by the symptoms of the problem.

Reference The component locator and schematic follow the "After-Repair Adjustments and Tests" table. Refer to figure 4-1 in Section IV for the location of cables and boards. Use the waveforms in table 8-42 as a reference for proper operation.

After-Repair Use table 8-43 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. There are three D/A converters on this board; two are used for conversion of digital data to analog signals and the third is used as an attenuator. The serial digital data must be clocked into the shift register and latched. If the problem seems to be in the digital circuits where it is difficult to analyze whether proper information is being received, check the signals used to clock and latch the data.
2. Some of the signals supplied by the calibrator circuits may be turned on with special beeper commands so that they stay on long enough to be analyzed thoroughly.
3. The only symptom of a defective overload circuit may be a burned out final amplifier. The overload protection could fail to protect the output amplifier or fail and **always** protect it. Since the first case is a failure that could remain hidden, it is recommended that the overload protection circuit be tested any time the final amplifier is found to be defective. The latter case would keep the source from putting out any signal which would be an obvious problem.

Sine Wave Circuitry Test

1. Use the following key strokes to turn on the source:

[Control]						
PRESET	......	RESET				
[Measurement]						
SOURCE	......	SOURCE TYPE	......	FIXED SINE	.....	**32** kHz
	......	SOURCE LEVEL	......	**5** V		

   The signal at TP11 should now appear as shown in the first waveform of table 8-42. This particular frequency is selected because it is a factor of the 256 kHz clock signal for the DAC, which allows the scope to synchronize. 64 kHz, 16 kHz, or 8 kHz would work as well.

2. Examine the waveforms along the signal path at test points TP5, TP15, and TP13 and compare them to waveforms in table 8-42. The signal amplitude at test points TP15 and TP13 (after the attenuator) should change with changes in the source level. Signal amplitudes at test points TP11 and TP5 (before the attenuator) do **not** change when the source level is changed.

3. The status of the attenuator control lines vary for different source level selections. Table 8-40 shows the status of each line for any given source level selection to aid in the isolation of attenuation problems between the shift registers (U500, U501, and U502) and the multiplying DAC (U251). Codes not in the table may be derived by dividing the desired voltage (source level) by 5 mV and converting the result from a decimal number to a binary number.

Table 8-40. Attenuator Data Input versus Source Output Level

Source Levels	TTL Levels (high or low)										Decimal
0 mV	0	0	0	0	0	0	0	0	0	0	0
10 mV	0	0	0	0	0	0	0	0	1	0	2
1 V	0	0	1	1	0	0	1	0	0	0	200
2 V	0	1	1	0	0	1	0	0	0	0	400
3 V	1	0	0	1	0	1	1	0	0	0	600
4 V	1	1	0	0	1	0	0	0	0	0	800
5V	1	1	1	1	1	0	1	0	0	0	1000
5.1 V	1	1	1	1	1	1	1	1	0	0	1020
U251 pin #	4	5	6	7	8	9	10	11	12	13	
data bit #	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	

DC Offset Test

1. To test the operation of the dc offset, select a dc offset on the front panel and measure the result at TP10. The reading should be of opposite polarity and half the selected value; e.g. if you select +1 V the reading should – 0.50 V ± 0.01 V.

2. If the readings are not as predicted, the failure is in the D/A converter (DAC) circuit or the digital circuitry previous to the DAC. Check the following digital signals for activity:
   - LDSRCL (load source, active low) latches data into U500 & U502. This signal appears only when changes are made via the front panel (such as changing dc offset or source level). A logic probe may be used to detect activity on this line.
   - CNTCLK (control clock) clocks serial data into the serial-to-parallel shift registers. Check this signal at the input of both U501 (pin 8) and U502 (pin 2). Data appears on this line only when changes are made from the front panel that cause a change in the status of these circuits, such as changing the dc offset or source level.
   - CNTLD (control data) is the serial data that is loaded into U500 and U502. Data appears on this line only when changes are made from the front panel that cause a change in the status of these circuits, such as changing the dc offset or source level.

Note

The source must be turned on by selecting one of the signal types. Selecting a source level of 0 V keeps signals from the sine wave interface circuitry from interfering with testing of the dc offset circuitry.

---

3. Move the voltmeter probe to TP13. The readings on this test point should coincide with the front panel dc offset selections within 10 mVrms when 0 V is selected and within 50 mV when 10 V is selected.

Calibration Circuits Test

These circuits include schematic blocks for the square wave and pseudo random noise sources, signal selection, and the calibrator. In normal operation these circuits are used only during calibration and are not controllable by the operator. These circuits may be controlled through the use of beeper commands as described in the following discussion.

Note

It does not matter whether the beeper is being turned on or off; pressing the key is all that is required to activate the command sequence. The beeper commands toggle the feature on and off; using it twice turns it on and then off.

If the measurement stops and the "WAITING FOR TRIGGER" message appears in the lower right hand part of the display, the measurement may be restarted by issuing the beeper command twice (calibration may interrupt without warning; auto cal may be turned off to prevent this).

If beeper commands have been activated the instrument must be reset before it can make measurements. This is required because the beeper commands configure internal circuits for special tests which do not allow accurate measurements to be made.

4 kHz Square Wave Calibration Circuits Test

This sequence of key strokes turns on the 4 kHz square wave in the calibrator, connects it to the analyzer front end, configures the trigger to run on the CALTRIG signal from the analog source board, and configures the display to show magnitude and phase with sideband markers on the significant frequencies.

Press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

[Input Setup]
SELECT
TRIG ...... MORE
TYPES ...... EXT
TRIG

[Measurement]
WINDOW ..... UNIFRM
(NONE)

[Input Setup]			
RANGE	**—13**	dBVrms	
[Control]			
SPCL FCTN	BEEPER ON/OFF	**—519**	ENTER (turns on 4 kHz sq wv)
[Display]			
A&B			
MEAS DISP	FILTRD INPUT	LINEAR SPEC 1	
[Markers]			
SPCL MARKER	SBAND ON	CRRIER FREQ	**52** kHz
		SBAND INCRMT	**8** kHz
[Display]			
B			
COORD	PHASE		
[Display]			
A&B			

The display of the HP 3563A should appear as shown in table 8-42, Waveform #3. The sideband markers (birds) in the phase trace should be stationary. Unstable phase components at these frequencies indicate a triggering problem. Waveform #4 shows the relationship between the output signal at TP8 and CALTRIG at pin 9 of U451.

64 kHz Square Wave Calibration Circuits Test

This sequence of key strokes turns on the 64 kHz square wave in the calibrator, connects it to the analyzer front end, configures the trigger to run on the CALTRIG signal of the analog source board, and configures the display to show magnitude and phase.

Press the HP 3563A keys as follows

⌈ Control ⌉
PRESET ...... RESET

⌈ Input Setup ⌉
SELECT
TRIG ...... MORE
TYPES ...... EXT
TRIG

⌈ Measurement ⌉
WINDOW ...... UNIFRM
(NONE)

⌈ Input Setup ⌉
RANGE ...... **—13** ...... dBVrms

⌈ Control ⌉
SPCL
FCTN ...... BEEPER ...... **—522** ..... ENTER
ON/OFF (64 kHz sq wv)

⌈ Display ⌉
A&B

MEAS
DISP ...... FILTRD
INPUT ...... LINEAR
SPEC 1

⌈ Display ⌉
B

COORD ...... PHASE

⌈ Display ⌉
A&B
X (turns on marker at peak magnitude; here it's at 64 kHz)

The display of the HP 3563A should appear as shown in table 8-42 A30, Waveform #5. The marker on the phase trace should be stationary. Unstable phase at this frequency indicates a triggering problem. Waveform #6 shows the relationship between the output signal at TP8 and CALTRIG at pin 9 of U451.

Pseudo Random Noise (PRN) Source Calibration Circuits Test

This sequence of key strokes turns on the PRN source in the calibrator, connects it to the analyzer front end, configures the trigger to run on the CALTRIG signal of the analog source board, and configures the display to show magnitude and phase with sideband markers on the significant frequencies. Any of the 100 frequencies may be analyzed by changing the carrier frequency; 90 kHz was selected because the upper frequencies are most sensitive to changes in phase.

Press the HP 3563A keys as follows:

[Control]
PRESET ..... **RESET**

[Input Setup]
SELECT TRIG ...... **MORE TYPES** ...... **EXT TRIG**

[Measurement]
WINDOW ...... **UNIFRM (NONE)**

[Input Setup]
RANGE ...... **—13** ...... **dBVrms**

[Control]
SPCL FCTN ...... **BEEPER ON/OFF** ...... **—514** ..... **ENTER** (turns on PRN)

[Display]
A&B

[Display]
MEAS DISP ...... **FILTRD INPUT** ...... **LINEAR SPEC 1**

⌈ Markers ⌉
SPCL
MARKER ...... SBAND ON ...... CRRIER FREQ ..... **90 kHz**
...... SBAND INCRMT ..... **1 kHz**

⌈ Display ⌉
B
COORD ...... PHASE

⌈ Display ⌉
A&B

The display of the HP 3563A should appear as shown in table 8-42, Waveform #7. The sideband markers (birds) in the phase trace should be stationary. Unstable phase components at these frequencies indicate a triggering problem. Waveform #8 shows the relationship between the output signal at TP8 and CALTRIG at pin 9 of U451.

Inverted Pseudo Random Noise (INV PRN) Source Calibration Circuits Test

This sequence of key strokes turns on the INV PRN source in the calibrator, connects it to the analyzer front end, configures the trigger to run on the CALTRIG signal of the analog source board, and configures the display to show magnitude and phase with sideband markers on the significant frequencies.

Press the HP 3563A keys as follows:

⌈ Control ⌉						
PRESET	......	RESET				
⌈ Input Setup ⌉						
SELECT						
TRIG	......	MORE				
		TYPES	......	EXT		
				TRIG		
⌈ Measurement ⌉						
WINDOW	......	UNIFRM				
		(NONE)				
⌈ Input Setup ⌉						
RANGE	......	**—13**	......	dBVrms		
⌈ Control ⌉						
SPCL						
FCTN	......	BEEPER	......	**—515**	.....	ENTER
		ON/OFF				(turns on INV PRN)
⌈ Display ⌉						
A&B						
MEAS						
DISP	......	FILTRD				
				INPUT	.....	LINEAR
						SPEC 1
⌈ Markers ⌉						
SPCL						
MARKER	......	SBAND				
		ON	......	CRRIER		
				FREQ	.....	**90 kHz**
			......	SBAND		
				INCRMT	.....	**1 kHz**

⌈ Display ⌉
B
COORD ...... PHASE

⌈ Display ⌉
A&B

The display of the HP 3563A should appear as shown in table 8-42, Waveform #9. The sideband markers (birds) in the phase trace should be stationary. Unstable phase components at these frequencies indicate a triggering problem. Waveform #10 shows the relationship between the output signal at TP8 and CALTRIG at pin 9 of U451.

If these special commands do not result in the proper signal appearing at TP8, check for proper operation of the signal selection circuits and the sources of the signals using table 8-41.

Note

The calibrator trigger signal for pseudo random noise is the same for either PRN or inverted PRN.

Table 8-41. Control Line Status versus Selected Signal

Control Line	Selected Signal			
	64 kHz	4 kHz	INV PRN	PRN
INV CAL U452(2)	L	L	H	H
SEL CAL U452(14)	L	H	L	H

Overload Detection Circuit Tests

This procedure tests all components necessary for overload protection including the comparators, the logic, the relay and the relay driver.

1. Connect a variable dc source to the source output connector on the front panel. Set the dc source output level to 0 V.
2. Monitor the voltage on the output side of A30 R404 with a voltmeter.
3. Increase the dc level and monitor the voltmeter reading. The reading should increase until it reaches 13 V ± 1 V and then fall to less than 1 V.
4. The error message"Source Fault" should appear in the lower right corner of the display.
5. To erase the error message, press the following keys:

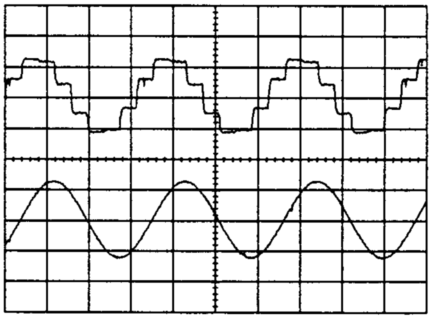
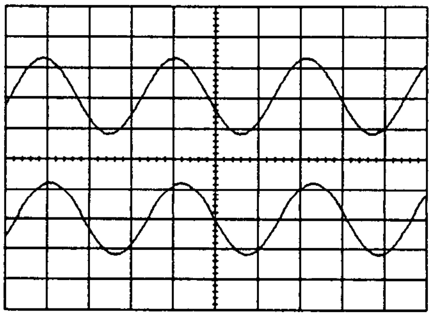
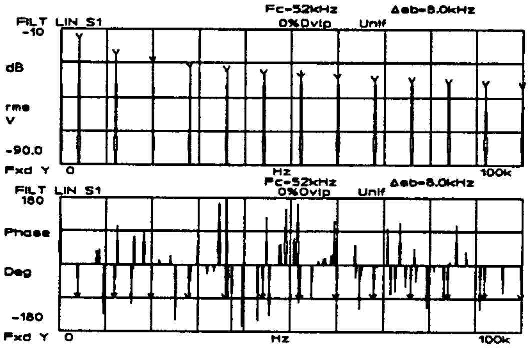
   [Control]
   PRESET ...... RESET

6. Reverse the polarity of the signal connected to the front panel source connector and repeat steps 2 through 4.

Waveform and Spectrum Plots

The following illustrations are display plots of measurements taken with the HP 3563A spectrum analyzer (used to look at signals within itself) and an oscilloscope. These waveforms are provided to aid in troubleshooting the analog source board, A30.

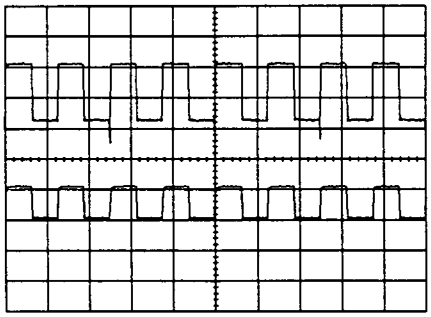
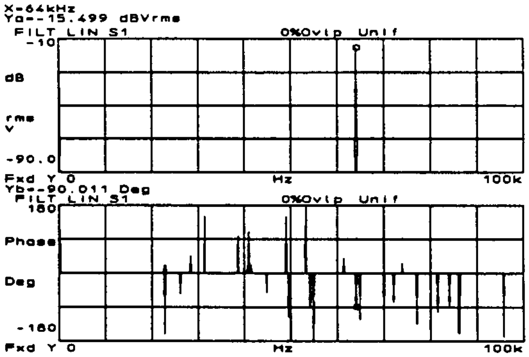
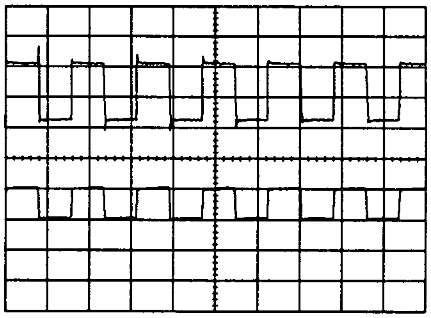
Table 8-42. Analog Source Signal Waveforms

<table>
<tr><td colspan="3">Remove power
Jumpers in normal (N) position
Probe type 1:1
Power on</td></tr>
<tr><td colspan="3">The key presses required to activate the signals shown are listed in the service procedures.</td></tr>
<tr><th>Setup</th><th>Parameters</th><th>Display</th></tr>
<tr><td>32 kHz sine signal at TP11 and TP5
Configure the instrument as described in the "Sine Wave Circuitry Test," step I.
CH1 scale 2.0 V/div
CH2 scale 2.0 V/div
Sweep at 10 μs/div</td><td>Waveshape and amplitude</td><td>
#1</td></tr>
<tr><td>32 kHz sine signal at TP15 and TP13
Configure the instrument as described in the "Sine Wave Circuitry Test," step I.
CH1 scale 2.0 V/div
CH2 scale 4.0 V/div
Sweep at 10 μs/div</td><td>Waveshape and amplitude</td><td>
#2</td></tr>
<tr><td>Calibrator 4 kHz square wave spectrum
Configure the instrument as described in the "4 kHz Square Wave Calibration Circuits Test."</td><td>Marker position</td><td>
#3</td></tr>
</table>

Analog Source Signal Waveforms continued

Remove power
Jumpers in normal (N) position
Probe type 1:1
Power on

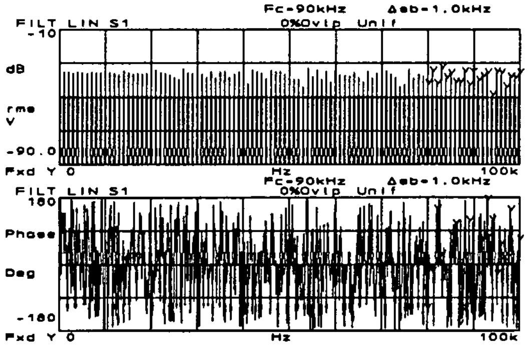
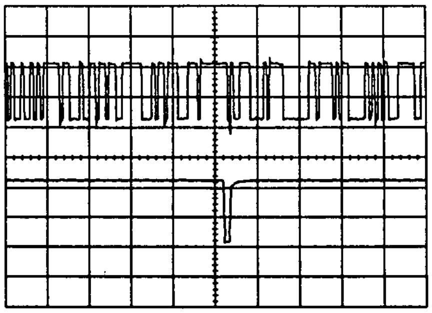
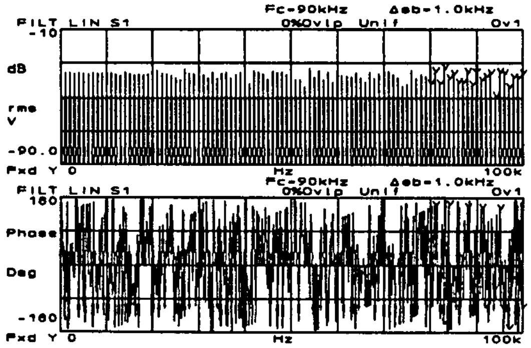
The key presses required to activate the signals shown are listed in the service procedures.

Setup	Parameters	Display
Calibrator 4 kHz square wave at TP8 and 4 kHz CALTRIG signal Configure the instrument as described in the "4 kHz Square Wave Calibration Circuits Test." CH1 scale 200 mV/div CH2 scale 4.0 V/div Sweep at 200 μs/div	Waveshape and amplitude	 #4
Calibrator 64 kHz square wave spectrum Configure the instrument as described in the "64 kHz Square Wave Calibration Circuits Test."	Marker position	 #5
Calibrator 64 kHz square wave at TP8 and 64 kHz CALTRIG signal Configure the instrument as described in the "64 kHz Square Wave Calibration Circuits Test." CH1 scale 200 mV/div CH2 scale 4.0 V/div Sweep at 10 μs/div	Waveshape and amplitude	 #6

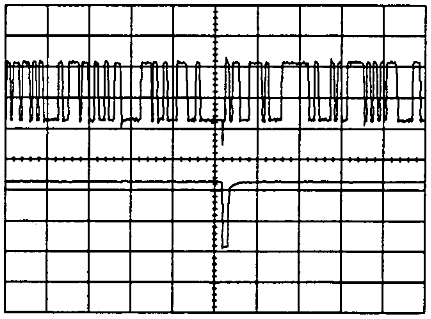
Analog Source Signal Waveforms continued

Remove power
Jumpers in normal (N) position
Probe type 1:1
Power on

The key presses required to activate the signals shown are listed in the service procedures.

Setup	Parameters	Display
Calibrator PRN Configure the instrument as described in the "PRN Source Calibration Circuits Test."	Magnitudes of spectra Phase markers should not move around	 #7
Calibrator PRN at TP8 and PRN CALTRIG signal Configure the instrument as described in "PRN Source Calibration Circuits Test." CH1 scale 200 mV/div CH2 scale 4.0 V/div Sweep at 50 μs/div (signal averaged to reduce noise)	Waveshape and amplitude	 #8
Calibrator inverted PRN spectrum Configure the instrument as described in the "INV PRN Source Calibration Circuits Test."	Magnitudes of spectra Phase markers should not move around	 #9

Analog Source Signal Waveforms continued

Remove power Jumpers in normal (N) position Probe type 1:1 Power on		
The key presses required to activate the signals shown are listed in the service procedures.		
Setup	**Parameters**	**Display**
Calibrator inverted PRN at TP8 and inverted PRN CALTRIG signal Configure the instrument as described in the "INV PRN Source Calibration Circuits Test." CH1 scale 200 mV/div CH2 scale 4.0 V/div Sweep at 50 μs/div (signal averaged to reduce noise)	Waveshape and amplitude	 #10

Analog Source After-Repair Adjustments and Tests

Table 8-43. After-Repair Adjustments and Tests

Perform the following:*	Section
Diagnostic Tests: SOURCE FUNCTN TEST ALL	VII
Adjustments: Source dc Offset Calibrator Gain	III
Performance Tests: Source Residual Offset Source Amplitude Accuracy and Flatness Source Distortion	II (Chapter 4, *HP 3563A Installation Guide*)
Operational Verification: Source Amplitude Accuracy and Flatness Single Channel Phase Accuracy	II (Chapter 3, *HP 3563A Installation Guide*

*Return all jumpers to the normal (N) position.

REFERENCE TABLE

IC	GND	+5V	V+	V-	+15V	-15V
U350					7(C352)	4
U351	5,12				7(C308)	3(C350)
U352					1,2(C356)	6,7(C357)
U451	7	14(C450)				
U452	15,8	16				
U455	7	14(C452)				
U500	10	20(C500)				
U501	7	14(C501)				
U502	12,13	24(C502)				
U550	8	16(C550)				
U551	8	16(C551)				
U552	10,19 2,3	20(C553)				
U553	10,19 2,3	20(C552)				
U1			7(C3)	4(C4)		
U2			7(C10)	4(C11)		
U150			7(C150)	4(C151)		
U151	7		14	8		
U250			7(C252)	4(C253)		
U300			7(C302)	4(C303)		
U301	1		13(C304)	3(C305)		
U400			7(C400)	4(C401)		
U401			11(C403)	7(C404)		
U504			7(C50)	4(C51)		
U600			11(C601)	6(C602)		

A30 Analog Source Ground and Power Chart

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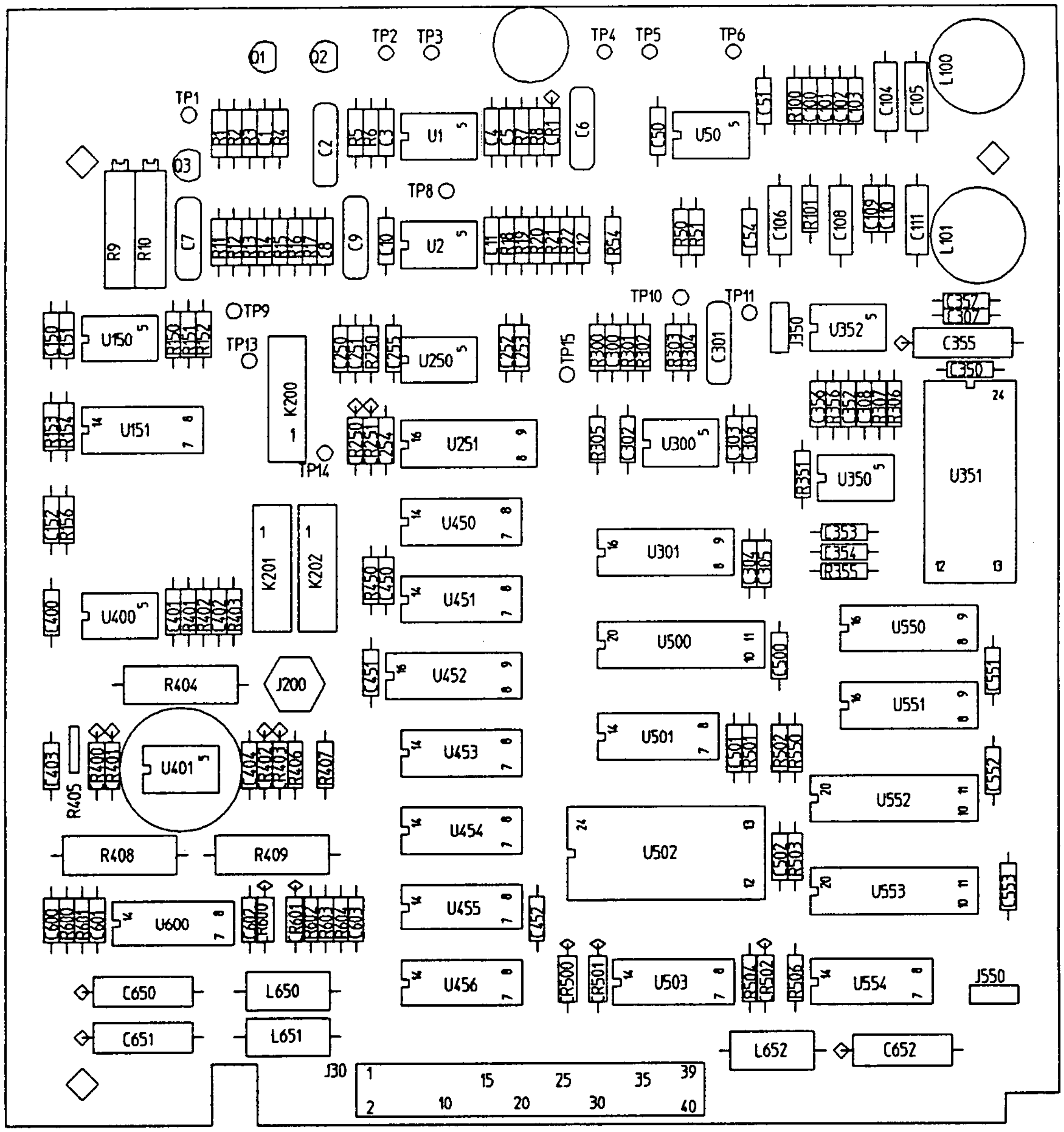

A30 Analog Source Component Locator
P/N 03562-66530 Rev C
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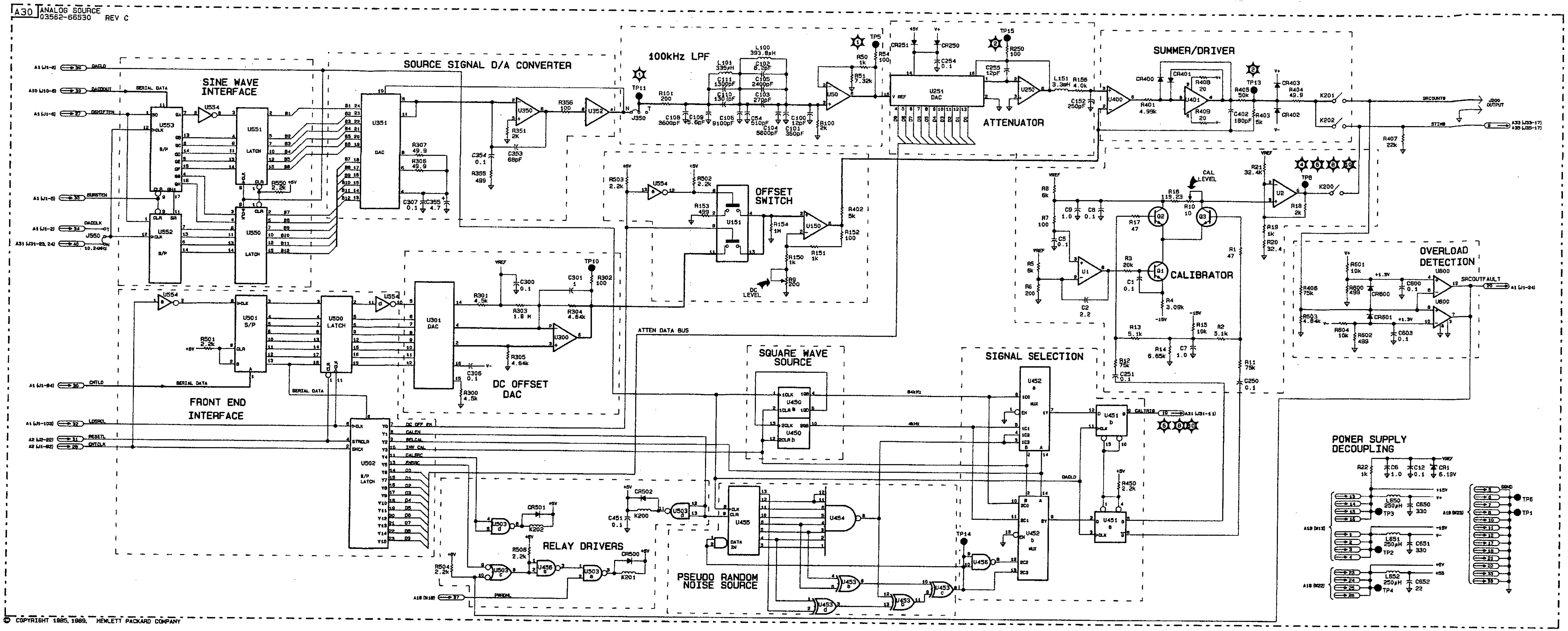

A30 Analog Source Schematic
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A31
Trigger

A31 Trigger

The information in this section should be used to isolate faulty subblocks in the A31 Trigger assembly. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the circuit descriptions of Section VI are understood.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Caution Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	Start troubleshooting by using figure 8-13. This procedure diagram describes the best order to perform the troubleshooting tests based on the symptoms observed.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
Verify	Use the oscilloscope waveforms in table 8-49 to see correct operation at various test points in the assembly.
After-Repair	Use table 8-50 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. In the VCXO subblock the most likely components to fail are Y401, CR402, CR403, Q401, and Q402. C406, C407, and L401 are critical components but are less likely to fail.
2. Trigger problems can be caused by the A1 Digital Source, the A6 Digital Filter Controller, the A30 Analog Source, the A31 Trigger, or the A32, A34 ADCs. Use the "Isolating Trigger Failures" procedure in Section VII to determine which assembly is failing.

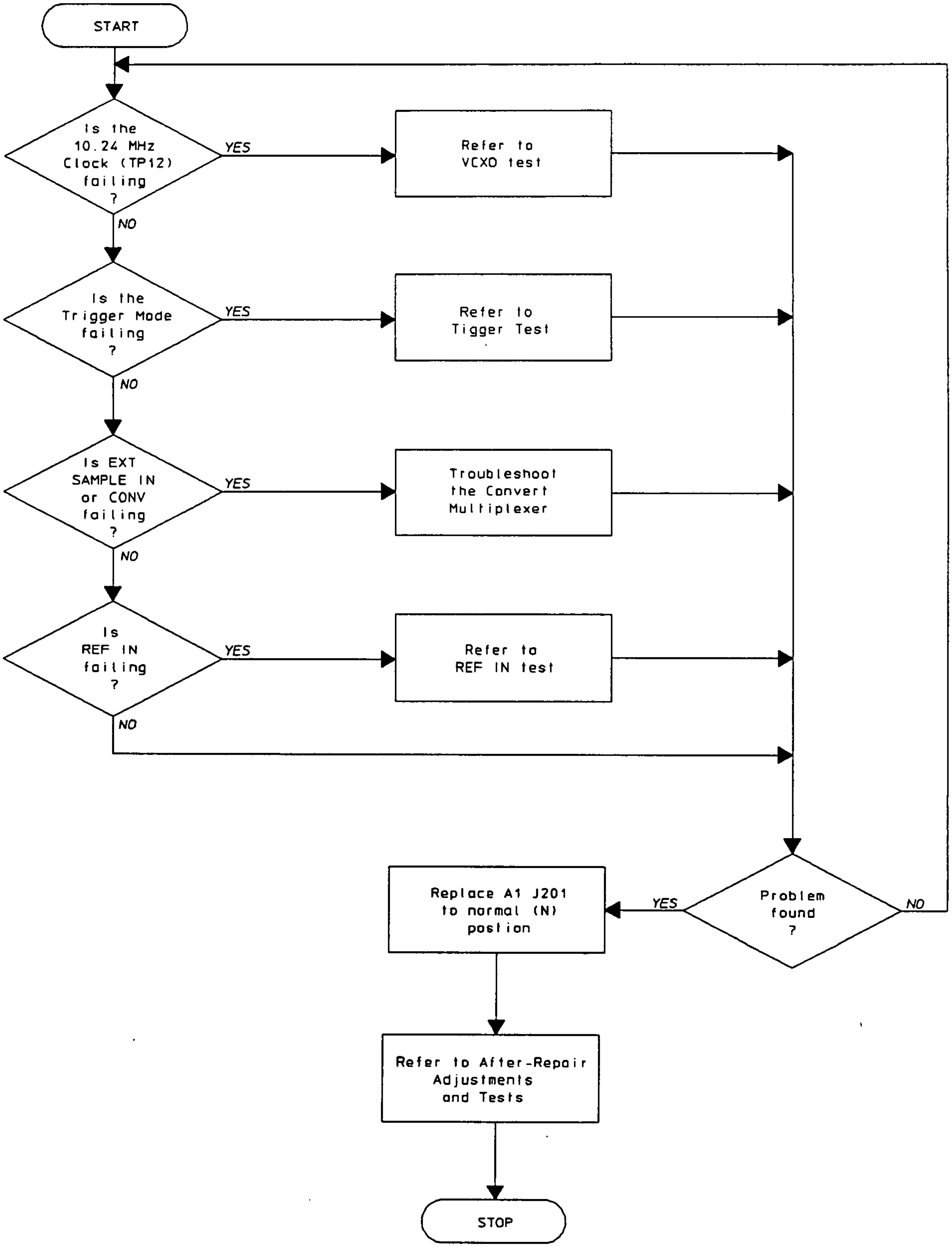

START
Is the 10.24 MHz Clock (TP12) failing ?
YES
Refer to VCXO test
NO
Is the Trigger Mode failing ?
YES
Refer to Tigger Test
NO
Is EXT SAMPLE IN or CONV failing ?
YES
Troubleshoot the Convert Multiplexer
NO
Is REF IN failing ?
YES
Refer to REF IN test
NO
Problem found ?
YES
NO
Replace A1 J201 to normal (N) postion
Refer to After-Repair Adjustments and Tests
STOP

Figure 8-13. A31 Trigger Troubleshooting Procedure Diagram

VCXO Test

1. Press the line switch OFF and remove the top cover. Place the A31 Trigger assembly on the extender board.
2. Press the line switch ON.
3. Use table 8-44 to isolate the failure.

Table 8-44. VCXO Test

Signal	Test Location	Waveform Number or Value
10.24 MHZ	A31 TP12	#1
20.24 MHZ	A31 TP10	#2
SMP OUT	A31 TP17 (U9-7)	#3
Control Voltage	A31 TP11	≅ – 4 to –6 Vdc
dc Adjustment Range	A31 R410	0 to + 10 Vdc
—	A31 R403	+5.5 ± 0.6 Vdc
—	A31 R408	+5.3 ± 0.8 Vdc
—	A31 U201-1	≅ – 1 to –1 5 Vdc

Trigger Test

1. Press the line switch OFF and remove the top cover. Place the A31 Trigger assembly on the extender board.
2. Press the line switch ON.
3. Perform steps 4 through 9 and use table 8-45, table 8-46, and table 8-47 to isolate the failure.
4. Connect a 5 Vpp, 1 kHz sine wave to the front panel EXT TRIGGER input.
5. To use table table 8-45 press the keys as follows:

[Control]
PRESET ...... RESET

[Input Setup]
SELECT
TRIG ...... TRIG
LEVEL ...... 1 V

...... SLOPE
±−

...... MORE
TYPES ...... EXT
TRIG

Note

TTL low is represented by a "0". TTL level high is represented by a "1".

Table 8-45. Trigger Test # 1

Signal	Test Location	Waveform Number or Value
Trigger Input	A31 TP1,A31 TP3	#5
DAC	A31 TP2	+ 0.14 ± 0.02 Vdc
Shift Register	A31 U4 pin 13	0
	14	0
	15	0
	16	1
	17	0
	18	0
	19	0
	20	1
	21	0
	22	1
	23	1
Decoder	A31 U3 pin 4	0
	5	1
	6	1
	7	1

6. Connect a 5 Vpp, 1 kHz sine wave to the front panel Channel 1 input.
7. To use table 8-46, press the HP 3563A keys as follows:

[Input Setup]
SELECT
TRIG ...... CHAN 1
INPUT

...... SLOPE
+− ...... TRIG
LEVEL ...... **0 V**

Table 8-46. Trigger Test # 2

Signal	Test Location	Waveform Number or Value
Trigger Input	A31 TP3,A31 TP1	#6
Shift Register	A31 U4 pin 13	0
	14	0
	15	1
	16	0
	17	1
	18	1
	19	1
	20	1
	21	1
	22	1
	23	0
Decoder	A31 U3 pin 4	1
	5	0
	6	1
	7	1

8. Connect a 5 Vpp, 1 kHz sine wave to the front panel Channel 2 input.
9. To use table 8-47, press the HP 3563A keys as follows:

[Input Setup]
SELECT
TRIG ...... CHAN 2
INPUT ...... SLOPE
± −
...... TRIG
LEVEL ...... 2 V

Table 8-47. Trigger Test # 3

Signal	Test Location	Waveform Number or Value
Trigger Input	A31 TP3	A31 TP1
Decoder	A31 U3 pin 4	1
	5	1
	6	0
	7	1

REF IN Test

1. Press the line switch OFF and remove the top cover. Place the A31 Trigger assembly on the extender board.
2. Press the line switch ON.
3. Connect a 0.1 Vrms, 1 MHz sine wave to the rear panel REF IN input.
4. Use table 8-48 to isolate the failure.

Table 8-48. REF IN Test

Signal	Test Location	Waveform Number or Value
REF IN / 125	A31 TP15 (U305-11)	#8
REF IN/ 3	A31 TP18 (U303-8)	#9
3.413 MHz	A31 TP16 (U507-5)	#10
80 kHz Filter	A31 U101-7	#11
Error Voltage	A31 TP6	0 ± 0.04 Vdc
UNLOCK	A31 TP9	TTL level low
Control Voltage	A31 TP11	– 4.0 ± 3 Vdc
Change REF IN frequency to 1.0002 MHz		
Control Voltage	A31 TP11	–10 ± 4 Vdc
Frequency Out	A31 TP10	20.484096 MHz
Change REF IN frequency to 2 MHz		
REF IN/ 3	A31 TP18 (U303-8)	#12
Change REF IN frequency to 5 MHz		
REF IN / 3	A31 TP18 (U303-8)	#13
Change REF IN frequency to 10 MHz		
REF IN/ 3	A31 TP18 (U303-8)	#14

Trigger Assembly Waveforms

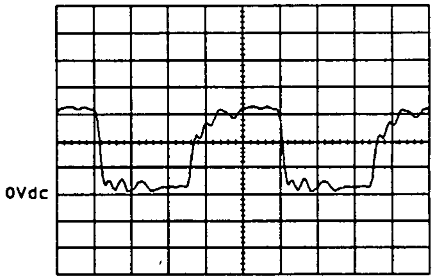
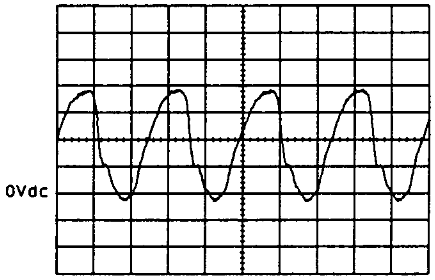
The oscilloscope plots are used for troubleshooting the A31 Trigger assembly. Note that all the measurements are taken with a **10:1** probe. Other notes unique to a measurement are written next to the waveform.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

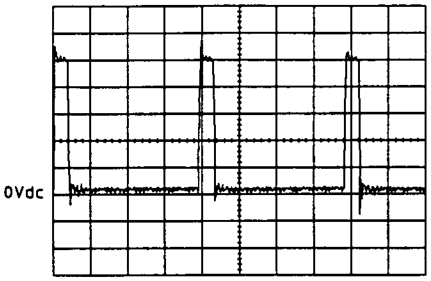
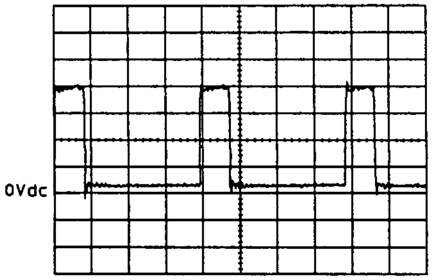
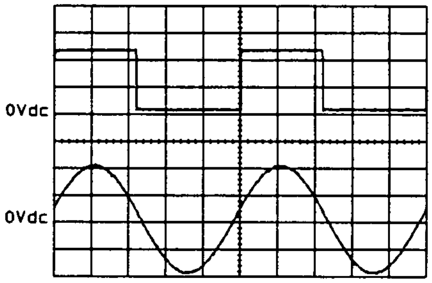
Table 8-49. Trigger Assembly Waveforms

All Jumpers should be in normal position
Connect ground to A31 TP7
Probe type 10:1

Setup	Parameters	Waveform
10.24 MHz Connect CH1 to A31 TP12 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 20 ns/Div Trigger CH 1	Time	 **#1**
20.48 MHz Connect CH1 to A31 TP10 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 20 ns/Div Trigger CH 1	Time	 **#2**

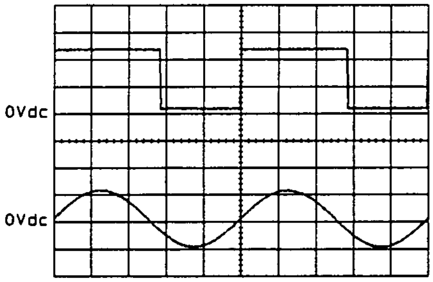
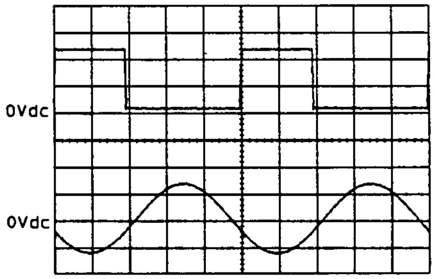
Trigger Assembly Waveforms continued

All jumpers should be in normal position
Connect ground to A31 TP7
Probe type 10:1

Setup	Parameters	Waveform
SMP OUT Connect CH1 to A31 TP17 (A31 U9-7) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 μs/Div Trigger CH 1	Time	 #3
CONV Connect CH1 to A31 U502-8 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 μs/Div Trigger CH 1	Time	 #4
Refer to "Trigger Test" for the HP 3563A input and key press		
EXT TRIG (Level = 1V) Connect CH1 to A31 TP3 Connect CH2 to A31 TP1 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 40 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 200 μs/Div Trigger CH 1	Time Relationship	 #5

Trigger Assembly Waveforms continued

Connect ground to A31 TP7
Refer to "Trigger Test" for the HP 3563A input and key presses.

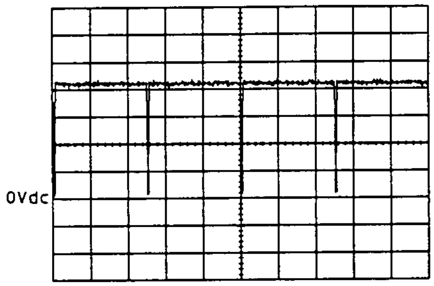
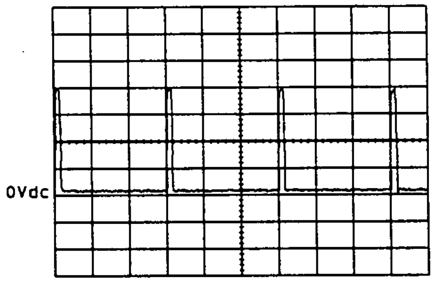
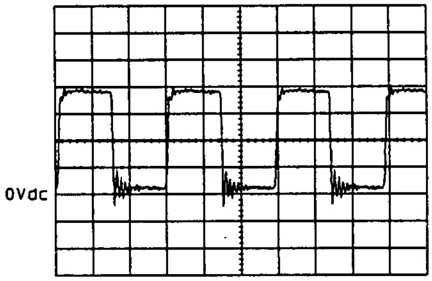
Setup	Parameters	Waveform
CHAN 1 TRIG (Level = 0V) Connect CH1 to A31 TP3 Connect CH2 to A31 TP1 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 100 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 200 μs/Div Trigger CH 1	Time Relationship	 **#6**
CHAN2 TRIG (Level = 2V) Connect CH1 to A31 TP3 Connect CH2 to A31 TP1 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 100 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 200 μs/Div Trigger CH 1	Time Relationship	 **#7**

Press A2 S1 (reset switch on the A2 CPU) after viewing the waveforms.

Trigger Assembly Waveforms continued

All jumpers should be in normal position
Connect ground to A31 TP7
Probe type 10:1

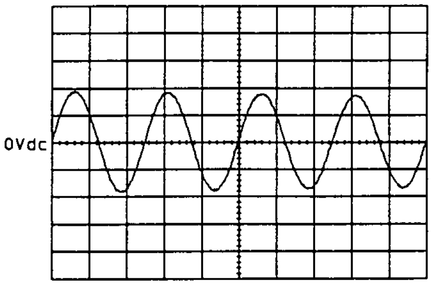
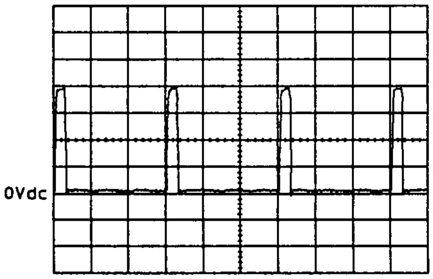
Refer to "REF IN Test" for the HP 3563A input and key presses.

Setup	Parameters	Waveform
REF IN / 125 (1 MHz REF IN) Connect CH1 to A31 TP15 (A31 U305-11) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 50 µs/Div Trigger CH 1	Time Note: Duty cycle varies with board Rev.	 #8
REF IN 13 (1 MHz REF IN) Connect CH1 to A31 TP18 (A31 U303-8) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 1 µs/Div Trigger CH 1	Time	 #9
3.413 MHz (1 MHz REF IN) Connect CH1 to A31 TP16 (A31 U507-5) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 100 ns/Div Trigger CH 1	Time	 #10

Trigger Assembly Waveforms continued

All jumpers should be in normal position
Connect ground to A31 TP7
Probe type 10:1

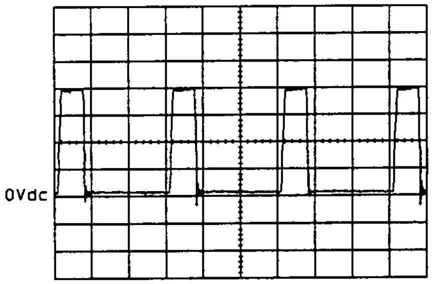
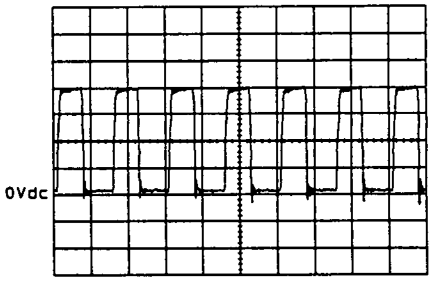
Refer to "REF IN Test" for the HP 3563A input and key presses.

Setup	Parameters	Waveform
80 kHz Filter (1 MHz REF IN) Connect CH1 to A31 TP16 (A31 U101-7) Oscilloscope: CH1 V/Div 50 mV/Div CH1 Coupling dc Time/Div 5 μs/Div Trigger CH 1	Time	 #11
REF IN / 3 (1 MHz REF IN) Connect CH1 to A31 TP16 (A31 U303-8) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 500 ns/Div Trigger CH 1	Time	 #12

Trigger Assembly Waveforms continued

All jumpers should be in normal position
Connect ground to A31 TP7
Probe type 10:1

Refer to "REF IN Test" for the HP 3563A input and key presses.

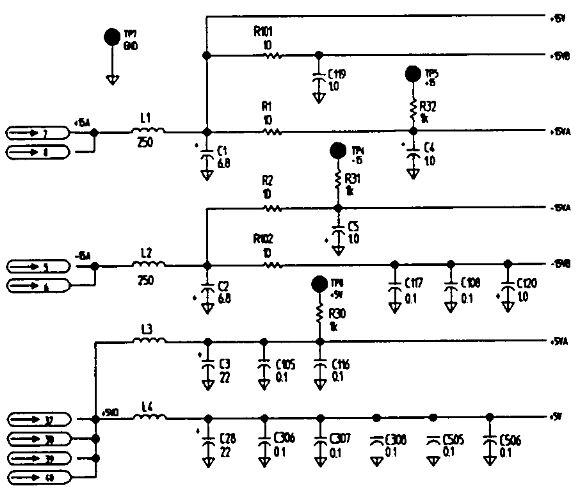
Setup	Parameters	Waveform
REF IN / 3 (5 MHz REF IN) Connect CH1 to A31 TP18 (A31 U303-8) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 200 ns/Div Trigger CH 1	Time	 **#13**
REF IN /3 (10 MHz REF IN) Connect CH1 to A31 TP18 (A31 U303-8) Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 200 ns/Div Trigger CH 1	Time	 **#14**

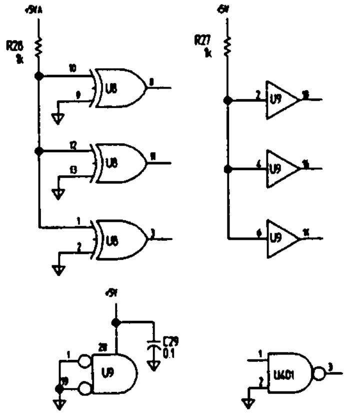
Trigger After-Repair Adjustments and Tests

Table 8-50. After-Repair Adjustments and Tests

Perform the following:	Section
Diagnostic Tests: TESTALL	VII
Adjustments: 20.48 MHz Reference	III
Performance Tests: None	II
Operational Verification: Frequency Accuracy Single Channel Phase Accuracy	II (Chapter 3, *HP 3563A Installation Guide*)

POWER SUPPLY DECOUPLING





REFERENCE TABLE

IC	+15VB	-15VB	+15VA	-15VA	+5VA	+5V	GND
U1			7(C10)	4(C11)			
U2			12(C14)	5(C13)			4
U3					16(C15)		10,13,16
U4					24(C30)		13,12
U5			7(C17)	4(C18)			
U6			13(C20)	3(C21)			1
U7					14(C24)		10
U8					14(C27)		
U101	8(C119)	4(C122)					
U201	4(C203)	8(C204)					
U301					14(C306)		10
U303							12,8
U304							3,4,6
U305						14(C305)	3,4,5 8
U401					14(C412)		
U501						14(C509)	
U502						14(C502)	
U503						14(C503)	
U504						14(C504)	
U507						14(C507)	
U508						14(C508)	7

A31 Trigger Ground and Power Chart
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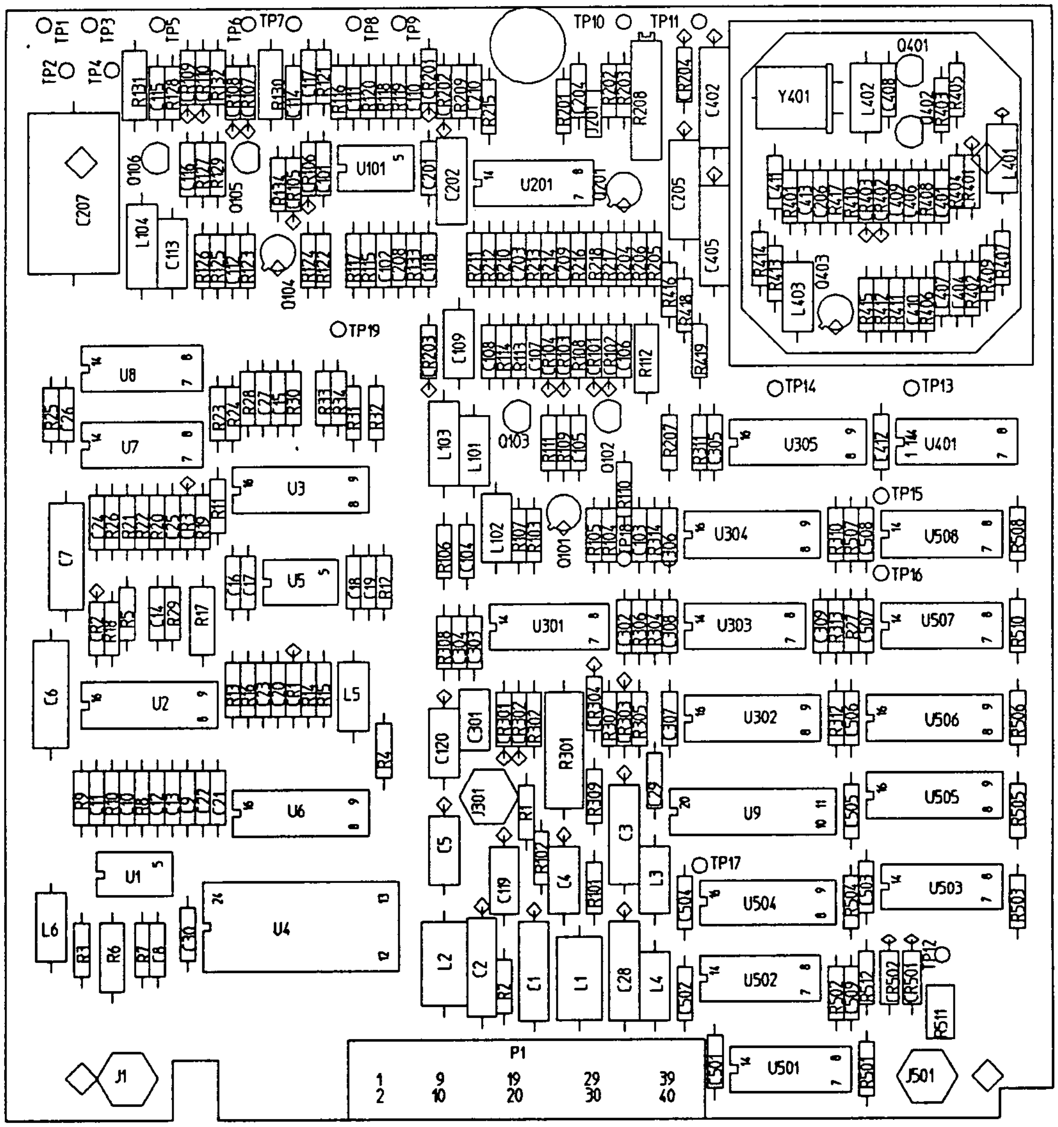

A31 Trigger Component Locator

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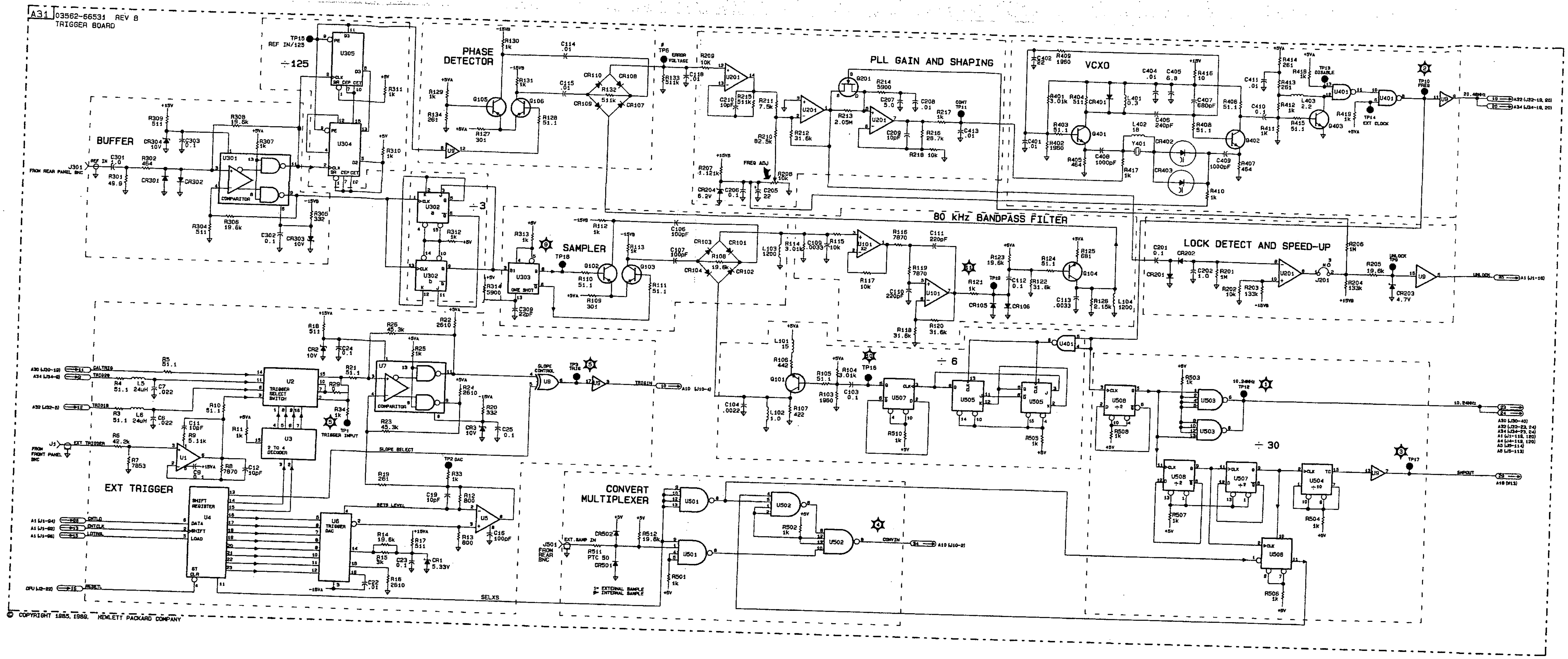

A31 Trigger Schematic
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A32, A34
ADC

A32, A34 Analog-to-Digital Converter (ADC)

The information in this section should be used to isolated faulty functional subblocks when servicing the HP 3563A. All procedures assume that you have used the Fault Isolation procedures in Section VII to determine this board has failed, and that you understand the Circuit Descriptions in Section VI.

Warning **Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).**

Caution Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start Three signals must be present for the ADC board to operate correctly. Check for the presence of the following signals:

1. 20.48 MHz clock at TP601
2. 10.24 MHz clock at TP607
3. 256 kHz (the CONVert signal) at TP600

All these signals are TTL and originate on the trigger board.

Compare Signals on the A32 board can be compared with signals on the A34 board since these boards are identical.

Reference The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.

After-Repair Use table 8-55 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. The trigger board and the corresponding input board must be installed when power is applied so that the serial data (control data signal CNTLDAD) signal path is complete.
2. The A/D conversion process on both boards is controlled by the ADC board in Channel Two (A34). See the discussion on master/slave selection in the circuit descriptions under the ADC board.

Signal Amplitudes vs Selected Range Test

This test may be used to check amplitudes of signals between amplifiers in the front end. Five ranges are given with a corresponding input signal level for each test point to thoroughly explore the operation of the range setting circuitry. Note that one of the check points is on the input board.

1. Disconnect the power cord from the rear panel and remove the top cover. Place the board to be checked on the extender board.
2. Connect the power cable and press the line switch on.
3. Connect a sine wave signal source to the front panel connector of the failing channel.
4. Press the HP 3563A keys as follows:

   [Control]
   PRESET ...... RESET

5. For each of the range settings in table 8-51 perform the following steps:

   a. Set the signal source's amplitude to the input amplitude shown in the table.

   b. Enter the corresponding range as follows:

   [Input Setup]
   RANGE ...... enter the range setting in table

   c. Use a voltmeter or scope to measure the voltage values at each test point listed in the table.

   - If multiple ranges fail, check the operation of the serial shift registers (U603, U203 and U202) and the switches they control (U100 and U200). The shift registers may be checked by monitoring the serial data line for activity and then checking the parallel outputs of the registers for the proper TTL levels as shown in table 8-52. Data flows on the serial data line immediately after entering range information on the front panel. Serial data is clocked in at pin 14 and out at pin 9 of each shift register.
   - If the switches are being driven with the correct TTL levels for a given range but signal levels are not the same as shown in the table, troubleshoot the attenuator and amplifier circuits.

Table 8-51. Signal Amplitude versus Range Setting

		Range Setting (in dBV)				
		+9	0	−5	−36	−51
Input Signal Amplitude	(Vrms) (Vpk)	2.818 3.985	1.000 1.414	0.5623 0.7952	0.0158 0.0223	0.0028 0.0040
A33 TP400 Amp 2	(dBV) (Vrms) (Vpk)	− 11.9 0.254 0.359	− 13.9 0.202 0.286	− 5.92 0.506 0.716	− 17.9 0.127 0.180	− 32.0 0.025 0.035
A32 TP101 Amp 3	(dBV) (Vrms) (Vpk)	− 8.37 0.381 0.539	− 8.37 0.381 0.539	− 8.37 0.381 0.539	− 8.37 0.381 0.539	− 22.4 0.076 0.108
A32 TP100 Amp 4	(dBV) (Vrms) (Vpk)	− 12.8 0.228 0.322	− 12.8 0.228 0.322	− 12.8 0.228 0.322	− 12.8 0.228 0.322	− 12.8 0.228 0.322

Note

All signal amplitudes listed have a tolerance of ± 5%.

Table 8-52. Range Setting vs Attenuator Setting

Range Setting	Attenuation	Atten #2 (A32 U200) pins (15)	(16)	(1)
– 51 to – 36 dBV	0 dBV	1	0	0
– 35 to – 34 dBV	2 dBV	1	0	1
– 33 to – 32 dBV	4 dBV	1	1	0
– 31 to – 30 dBV	6 dBV	1	1	1
– 29 to – 28 dBV	8 dBV	0	1	1
– 27 to – 26 dBV	10 dBV	0	1	0
– 25 to – 24 dBV	12 dBV	0	0	1
– 23 to – 22 dBV	2 dBV	1	0	1
– 21 to – 20 dBV	4 dBV	1	1	0
– 19 to – 18 dBV	6 dBV	1	1	1
– 17 to – 16 dBV	8 dBV	0	1	1
– 15 to – 14 dBV	10 dBV	0	1	0
– 13 dBV	12 dBV	0	0	1
– 12 dBV	4 dBV	1	1	0
– 11 to – 10 dBV	6 dBV	1	1	1
– 9 to – 8 dBV	8 dBV	0	1	1
– 7 to – 6 dBV	10 dBV	0	1	0
– 5 to – 4 dBV	12 dBV	0	0	1
– 3 to – 2 dBV	2 dBV	1	0	1
– 1 to 0 dBV	4 dBV	1	1	0
+ 1 to + 2 dBV	6 dBV	1	1	1
+ 3 to + 4 dBV	8 dBV	0	1	1
+ 5 to + 6 dBV	10 dBV	0	1	0
+ 7 dBV	12 dBV	0	0	1
+ 8 dBV	4 dBV	1	1	0
+ 9 to + 10 dBV	6 dBV	1	1	1
+ 11 to + 12 dBV	8 dBV	0	1	1
+ 13 to + 14 dBV	10 dBV	0	1	0
+ 15 to + 16 dBV	12 dBV	0	0	1
+ 17 to + 18 dBV	2 dBV	1	0	1
+ 19 to + 20 dBV	4 dBV	1	1	0
+ 21 to + 22 dBV	6 dBV	1	1	1
+ 23 to + 24 dBV	8 dBV	0	1	1
+ 25 to + 26 dBV	10 dBV	0	1	0
+ 27 dBV	12 dBV	0	0	1

Table 8-53. Range Setting vs Attenuator Setting

Range Setting	Attenuation	Atten #3 (A32 U100) pins		
– 51 to – 50 dBV	0 dBV	1	0	0
– 49 to – 48 dBV	2 dBV	1	0	1
– 47 to – 46 dBV	4 dBV	1	1	0
– 45 to – 44 dBV	6 dBV	1	1	1
– 43 to – 42 dBV	8 dBV	0	1	1
– 41 to – 40 dBV	10 dBV	0	1	0
– 39 to – 38 dBV	12 dBV	0	0	1
– 37 to + 27 dBV	14 dBV	0	0	0

Note

Attenuator #1 is on the A33, A35 assemblies.

No Signal Through The Main Data Path

This problem is either analog or digital. The signal is analog up to the process switch (at test point T/H OUT). Check the signal at this test point with a scope (and a IV sine wave input on the channel under test). For frequencies at or below 100 kHz the signal should appear as a sine wave because the T/H sampling rate (256 kHz) is much higher than the signal frequency. At higher frequencies the hold part of the track and hold circuit begins to show on the wave form. If there is no signal at test point T/H OUT then the analog circuit path is defective. The problem can be isolated by checking the signal at test points TP101, TP100, TP300 and T/H IN. Refer to table 8-51 for range and amplitude settings and expected signal levels at each test point.

TRACK AND HOLD CIRCUIT

The track and hold circuit is between test points T/H IN and T/H OUT. Before troubleshooting this circuit, check for a 256 kHz pulse train at TP600 and on the gate of Q400. This signal makes the T/H circuit track when high and hold when low. T/H OUT is identical (though inverted) to T/H IN while the circuit is tracking. These two signals may be overlaid on an oscilloscope display for comparison (as shown in the circuit descriptions section of this manual). The dc offset should be 50 mV or less and overshoot should be minimal. If high frequency oscillations are present at test point T/H OUT then C319, C400, or R402 may be defective.

The circuitry beyond T/H OUT converts the analog signal to a digital pulse stream (serial data). U602 on the ADC board in Channel 2 controls this process on both ADC boards. If the digital control of the digitizing circuits on Channel 1 is not correct and switching the boards corrects the problem, troubleshoot the controller on the original Channel 2 board.

DIGITAL

Most of U602 and some of the logic used to configure the ADC board is tested by diagnostic tests which are run from the front panel (as described in the fault isolation section). If the analog circuits are operating correctly and the problem can be isolated to the ADC board (by exchanging it with the ADC board in the other channel) then something in the digital portion of the data path is probably defective. This includes U601 (A/D converter), U602 (ADC controller), U600 (D/A converter), U406 and its supporting circuitry (finds the error voltage for second pass), and U405 (the process switch).

Refer to figure 8-14. This is the waveform appearing at TP405 with a 1 kHz input to the front panel. There are three distinct signals present which represent the three conversions as described in the theory of operation.

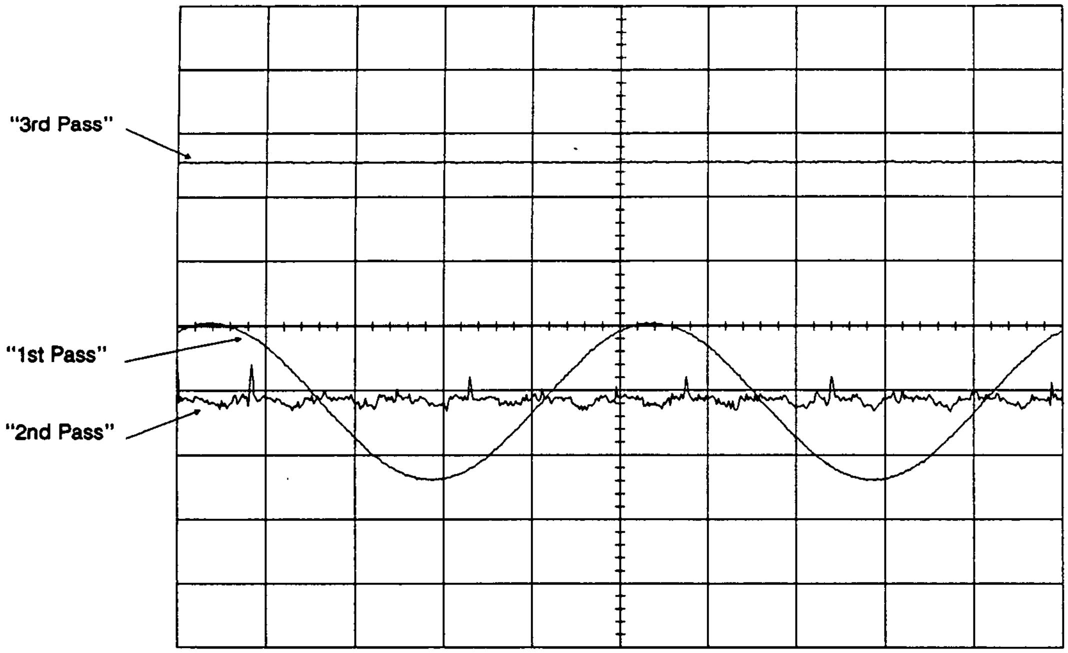


Figure 8-14. TP405 with a 1 kHz Input Signal

Distortion

A low distortion oscillator is required to troubleshoot distortion problems. Connect the oscillator output to the instrument input channel in question and view the results on the HP 3563A display. Harmonic distortion should be – 80 dB or less.

Distortion may be caused by problems on the input boards or the ADC boards. The circuits on these boards include input amplifiers, variable attenuators, the track and hold circuits, and the A/D converters. The problem may be isolated between an input board or ADC board by bypassing the input and injecting a signal at the input of the ADC board. The selected range and signal amplitude necessary is shown in table 8-54 (signal level appears in the ADC input column). Again, distortion should be less than – 80 dB and can be read from the instrument display. If there is no distortion when the input board is bypassed then troubleshoot the input board.

Distortion may be worse at one range setting than at others due to the various combinations of attenuator settings and the effective stress these combinations put on the different amplifier stages. Testing for distortion should be done such that the circuits being exercised are stimulated with a full scale signal. This varies from one stage to the next. Table 8-54 shows which stages are operating at maximum output level for a given range selection and corresponding signal level input.

Table 8-54. Range Settings and ADC Board Input Levels

Set Range (dBV)	Amp 1 out A33 TP601 (Vrms)	ADC input A33 TP400 (Vrms)	Amp 3 out A34 TP101 (Vrms)	Amp 4 out A34 TP100 (Vrms)	Amplifiers exercised
− 51	.0085	.0254	.0761	1.1477	4 only
− 37	.0424	.1271	.3814	1.1477	3 & 4
− 24	.1893	.5061	.3814	1.1477	2,3,& 4
− 13	.6716	.5061	.3814	1.1477	1,2,3,& 4
− 5	.1687	.5061	.3814	1.1477	2,3,& 4
+ 7	.6716	.5061	.3814	1.1477	1,2,3,& 4
+ 15	.1687	.5061	.3814	1.1477	2,3,&4
+ 27	.6716	.5061	.3814	1.1477	1,2,3,& 4

Notes :

- The test points for Amp 1 output and ADC input are on the input board.
- Use the range setting value as a source output level when the test signal is connected to the front panel (channel) inputs.
- ADC input = Amp 2 output, so when connecting the source directly to the ADC board use the levels listed in the ADC column.

Won't Trigger Off Individual Channel(s)

The signal used for triggering the instrument comes from the ADC board when Channel 1 or Channel 2 input triggering is selected. If the triggering works with an external trigger signal but not when individual channels are selected as the source of the trigger signal, then troubleshoot the path from TP100 through U501 to TP303.

Over Range and Half Scale Sensing Problems

Over range and half scale sensing are done by comparators U500 and U502. The signal from U501 drives the TRG@ line as well as these comparators. Problems with this circuit may be examined by using a dc source as an input signal and testing the operation of the comparator circuits. A quick check may be done by shorting the positive reference (+ 6.2R)to pin 5 of U502 and then shorting the negative reference (– 6.2R) to pin 9 of U500. Both the half scale and over range front panel LEDs should light when either connection is made. Keep in mind that the half scale output depends only on signals processed on the ADC board but the over range signal could be from the COVLD signal which is OR'd with the over range signal from the ADC board.

Offset D/A Converter

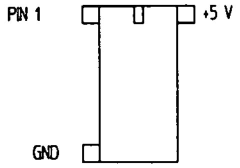
To determine whether an offset problem is in the data path components or the offset DAC, ground TP400 so that the DAC cannot provide any offset. With TP400 grounded there should be no more than 300 mV dc offset. If excessive offset is still present, the offset problem is in an amplifier circuit. If the offset is within limits with TP400 grounded, the offset problem may be U201, U202, or U203.

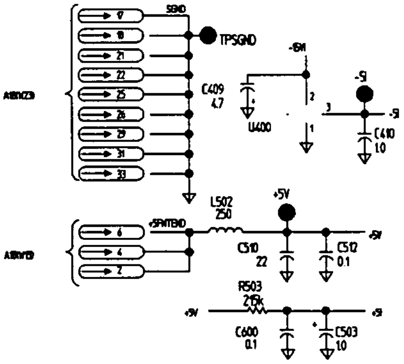
ADC After-Repair Adjustments and Tests

Table 8-55. After-Repair Adjustments and Tests

Perform the following:	Section
Diagnostic tests: TEST ALL	VII
Adjustments: Second pass gain ADC offset and reference Track and hold offset	III
Performance Tests: Amplitude Accuracy and Flatness	II (Chapter 4,*HP 3563A Installation Guide*)
Operational verification: Amplitude and Phase Match Single Channel Phase Accuracy Noise and Spurious Signal Level	II Chapter 3, *HP 3563A Installation Guide*

ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED TO PIN 8 AND +5 V IS CONNECTED TO PIN 16).





REFERENCE TABLE

IC	GND	+5V	-5V	+15A	-15A	+15B	-15B	+15C	-15C	+15D	-15D	+15E	-15E
U100	14											8	
U101												7(C101)	4(C100)
U102												7(C200)	4(C201)
U200	14											8	3
U201	1											8	
U202	8,13,9	16											
U203	8,10	16(C203)											
U300						7(C302)	4						
U301						7	4						
U401								7(C401)	4(C400)				
U402								7(C405)	4(C406)				
U403										8	4		
U404										7	4		
U405	8,4,11 12,13,16	16(C410)	-9										
U406										7	4		
U500	3,8			11	6								
U501				7(C501)	4(C500)								
U502	3,8			11	4(C503)								
U503		16(C540)											
U505	7	14											
U600	20	14,15,16											
U601	10(C600)	5?(C605)											
U602	10	5(C602)											
U603	8,13	16(C607)											
U604	1,10	20											

A32, A34 Analog-to-Digital Converter (ADC) Ground and Power Chart

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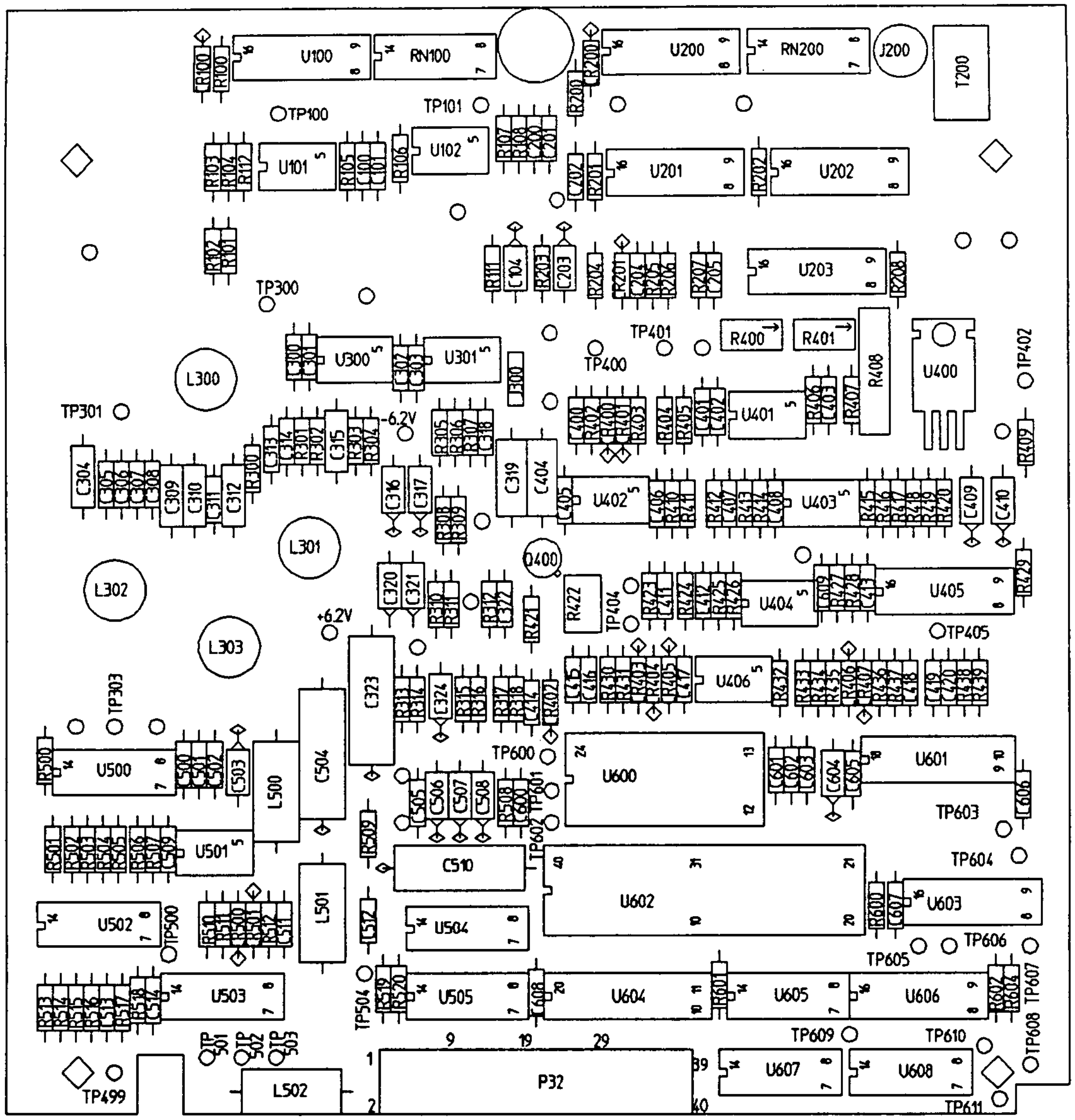

A32, A34 Analog-to-Digital Converter (ADC) Component Locator
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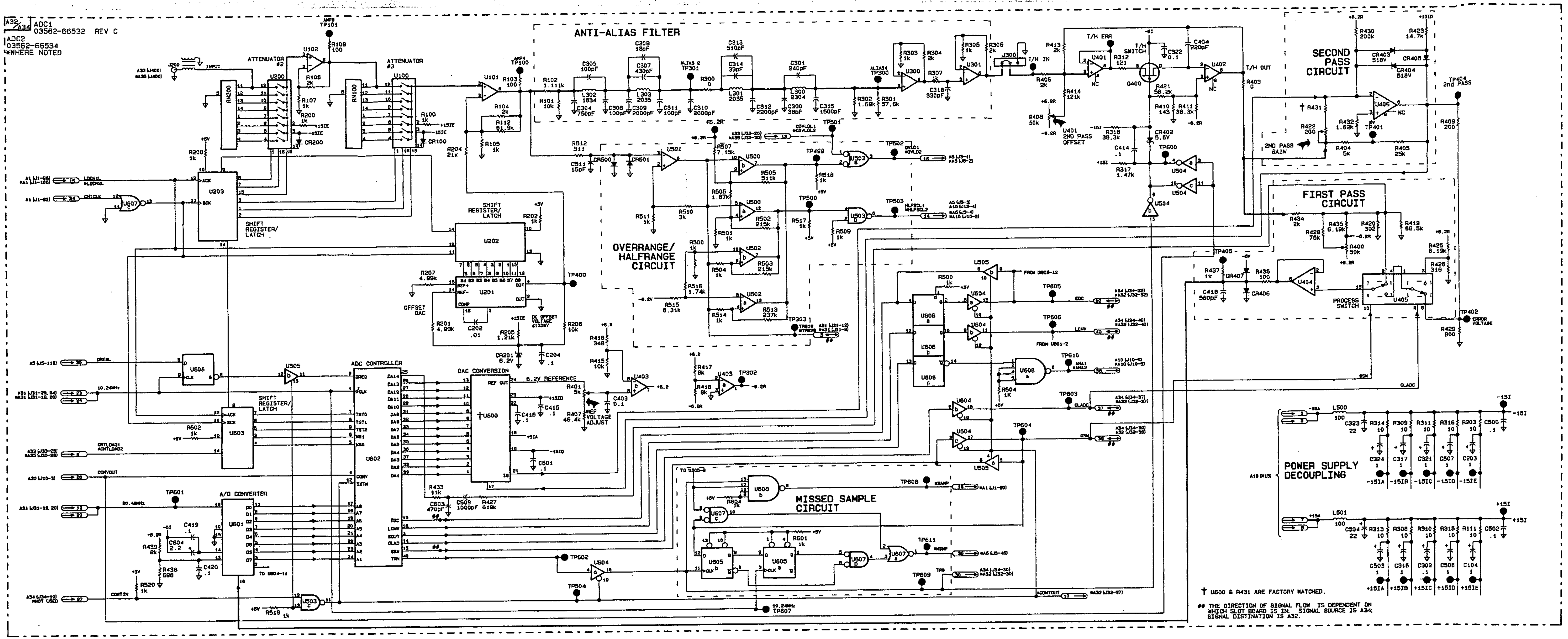

† U800 & R431 ARE FACTORY MATCHED.

THE DIRECTION OF SIGNAL FLOW IS DEPENDENT ON WHICH SLOT BOARD IS IN: SIGNAL SOURCE IS A34; SIGNAL DISTINATION IS A32.

A32, A34 Analog-to-Digital Converter (ADC) Schematic
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A33, A35
Input

A33, A35 Input

The information in this section should be used to isolate faulty subblocks in the A33 and A35 input assemblies. All procedures assume that you have used the Fault Isolation procedures in Section VII to determine this board has failed, and that you understand the Circuit Descriptions in Section VI.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury. Servicing must be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Caution

Do not insert or remove any circuit board in the HP 3563A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards. Many of the parts are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unneccessary damage.

How to Use This Section

Start	The primary method for troubleshooting the input assembly is to input a sine wave at A33 J300 and check the signal and voltage values at various test points in the circuit. Start with "Signal Amplitudes versus Range Setting Test". Use table 8-57 when a group of ranges are failing to determine most likely component failure.
Compare	Signals on the A33 board can be compared with signals on the A35 board since these boards are identical. Also, on each board the high input circuit and low input circuit are identical up to A33 TP600 and A33 TP500.
Reference	The component locator and schematic follow the "After-Repair Adjustments and Tests" table. For the location of cables and boards refer to figure 4-1 in Section IV.
Verify	Use table 8-56 to verify the input is operating correctly. Use the oscilloscope waveforms in table 8-58 to see correct operation of assembly.
After-Repair	Use table 8-59 to determine which adjustments and tests need to be done to complete instrument service.

Troubleshooting Hints

1. If all ranges are failing, check the relays and the shift registers.
2. If the voltage level at A33 TP501 is not correct, check the common mode rejection DAC subblock.

Signal Amplitudes Versus Range Setting Test

1. Disconnect the power cord from the rear panel and remove the top cover. Remove the cover shield MP401 and place the failing input board on the extender board.
2. Connect the extender cable to A33 J300.
3. Connect the power cable and press the line switch ON.
4. Input a 1 kHz sine wave into the BNC input connector of the failing channel; high on pin 3 and ground on pin 1.
5. Press the HP 3563A keys as follows:

⌈ Control ⌉
PRESET ...... RESET

⌈ Input Setup ⌉
INPUT
CONFIG ...... GROUND
CHAN1 ...... GROUND
CHAN2

Table 8-56. Signal Amplitude vs Range Setting

All signal amplitudes listed have a tolerance of ± 5%.

		Range Setting (in dBV)				
		+ 9	0	-5	-36	-51
Input Signal Amplitude	(Vrms)	2.818	1.000	0.5623	0.0158	0.0028
	(Vpk)	3.985	1.414	0.7952	0.0223	0.0040
A33 TP601 Difference Amplifier	(dBV)	− 31.0	− 20.0	− 25.0	− 36.0	− 52.0
	(Vrms)	0.028	0.100	0.562	0.0158	0.0028
	(Vpk)	0.049	0.141	0.794	0.0223	0.0040
A33 TP402 Amp 1	(dBV)	− 21 5	− 10.5	− 15.5	− 26.5	− 41.5
	(Vrms)	0.085	0.300	0.169	0.047	0.0084
	(Vpk)	0.120	0.424	0.239	0.067	0.012
A33 TP400 Amp 2	(dBV)	− 11.9	− 13.9	− 5.92	− 17.9	− 32.0
	(Vrms)	0.254	0.202	0.506	0.127	0.025
	(Vpk)	0.359	0.286	0.716	0.180	0.035

6. For each of the range settings in table 8-56 perform steps a through d:

   a. Set the sine wave's amplitude to the input amplitude in the table.

   b. Press the HP 3563A keys as follows:

   [Input Setup]
   RANGE ...... To range setting in table

   c. Using a voltmeter or scope, measure the voltage values at each test point listed in the table.

   d. If the voltages values are correct, the high input side is most likely operating correctly.

7. To test the low input side, input a 1 kHz sine wave into the BNC input connector of the failing channel; high on pin 1 and ground on pin 3.

8. For each of the range settings in table 8-56 perform steps a through d:

   a. Set the sine wave's amplitude to the input amplitude in the table.

   b. Press the HP 3563A keys as follows:

   [Input Setup]
   RANGE ...... To range setting in table

   [Input Setup]
   INPUT
   COUPLE ...... FLOAT CHAN1

   ...... FLOAT CHAN2

   c. Using a voltmeter or scope, measure the voltage values at A33 TP601.

   d. If the voltages values are correct, the low input side is most likely operating correctly.

Range Setting vs. Attenuator Setting

Use table 8-57 when a group of ranges are failing to determine the most likely component failure.

Table 8-57. Range Setting vs Attenuator Setting

Range Setting	Attenuation	Component	
		High Input (BNC Center)	Low Input (BNC Shell)
– 51 to – 13 dBV	0 dBV	A33 K207	A33 K107
– 12 to 7 dBV	20 dBV	A33 K206 A33 K208	A33 K106 A33 K108
8 to27 dBV	40 dBV	A33 K205 A33 K209	A33 K105 A33 K109
		Attenuator #1 (A33 U401)	
		(16)	(1)
– 51 to – 25 dBV odd	0 dBV	0	0
– 50 to – 24 dBV even	1 dBV	0	1
– 23 to – 13 dBV odd	12 dBV	1	0
– 22 to – 14 dBV even	13 dBV	1	1
– 12 to – 4 dBV even	1 dBV	0	1
– 11 to – 5 dBV odd	0 dBV	0	0
– 3 to 7 dBV odd	12 dBV	1	0
– 2 to 6 dBV even	13 dBV	1	1
8 to 16 dBV even	1 dBV	0	1
9 to 15 dBV odd	0 dBV	0	0
17 to 27 dBV odd	12 dBV	1	0
18 to 26 dBV even	13 dBV	1	1

Attenuators #2 and #3 are on the A32, A34 assemblies

Input Assembly Waveforms

The oscilloscope plots are used for troubleshooting the A33, A35 input assemblies. Note that all the measurements are taken with a **10:1** probe. Other notes unique to a measurement are written next to the waveform.

To input a 1 kHz sine wave perform steps 1 through 5:

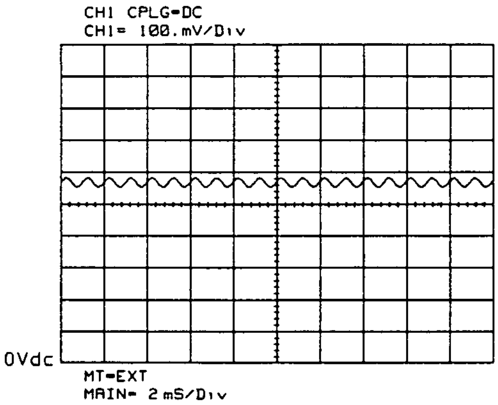
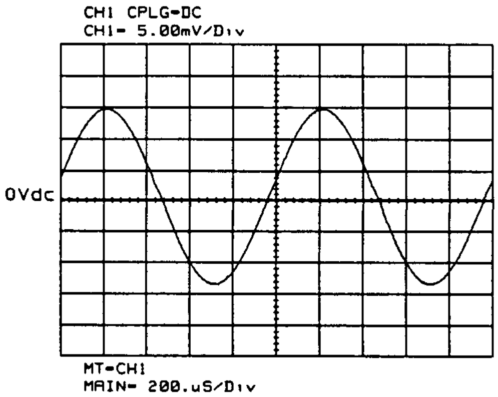
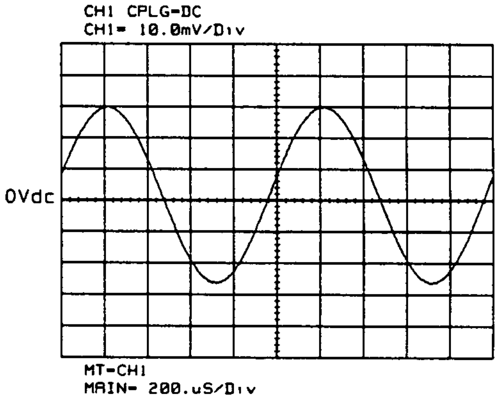
1. Disconnect the power cord from the rear panel and remove the top cover. Remove the cover shield MP401 and place the input board on the extender board.
2. Connect the extender cable to A33 J300.
3. Connect the power cable and press the line switch ON.
4. Input a 1 kHz sine wave with an amplitude of 1 Vrms into the BNC input connector of the failing channel. Terminate the signal at the front panel connector with a load that matches the signal source impedance.
5. Press the HP 3563A keys as follows:

[Control]
PRESET ...... RESET

[Input Setup]
RANGE ..... 1 Vrms

Table 8-58. Input Assembly Waveforms

Jumpers in test position: All Normal
Connect ground to A33 TP401
Probe type 10:1

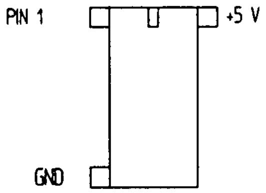
Setup	Parameters	Waveform
Bootstrap Circuit Connect CH1 to A33 U200-7 Oscilloscope: Mode A CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 2 ms/Div Trigger EXT ÷ 1, A33 J300-1	Waveshape Amplitude	 **#1**
TP601 Connect CH1 to A33 TP601 Oscilloscope: Mode A CH1 V/Div 5 mV/Div CH1 Coupling dc Time/Div 200 μs/Div Trigger CH 1	Waveshape Amplitude	 **#2**
TP400 Connect CH2 to A33 TP400 Oscilloscope: Mode A CH1 V/Div 10 mV/Div CH1 Coupling dc Time/Div 200 μs/Div Trigger CH 1	Waveshape Amplitude	 **#3**

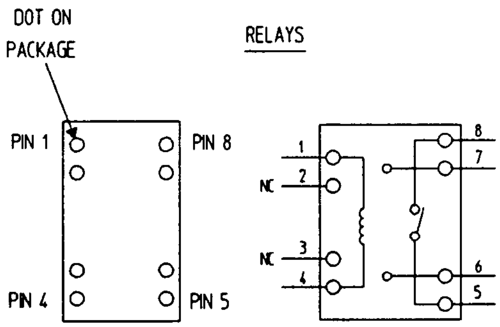
Input Assembly After-Repair Adjustments and Tests

Table 8-59. After-Repair Adjustements and Tests

Perform the following:	Section
Diagnostic Tests: FR END FUNCTION TEST ALL	VII
Adjustments: Input DC Offset Adjustment If a component in the input switches/attenuators subblocks was replaced perform the following adjustments: Input 40 dB Attenuator Adjustment Input 20 dB Attenuator Adjustment The input and ADC boards are adjusted in pairs. If an input or ADC board was switched perform the following adjustments: 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment Track and Hold Offset Adjustment Input DC Offset Adjustment Input Attenuator Adjustments	III
Performance Tests: Amplitude Accuracy and Flatness	II (Chapter 4, *HP 3563A Installation Guide)*
Operational Verification: Amplitude and Phase Match Common Mode Rejection Single Channel Phase Accuracy Noise and Spurious Signal Level	II (Chapter 3, *HP 3563A Installation Guide*)

ALL INTEGRATED CIRCUITS ARE CORNER POWERED EXCEPT THOSE SHOWN IN THE REFERENCE TABLE.CORNER POWERED ICs HAVE GROUND CONNECTED TO THE LOWER LEFT PIN, AND +5 V CONNECTED TO THE UPPER RIGHT PIN,REGARDLESS OF THE TOTAL PIN COUNT (e.g.,FOR A 16 PIN DIP, GROUND IS CONNECTED TO PIN 8 AND +5 V IS CONNECTED TO PIN 16).





SCHEMATIC COAXIAL
SHIELD TERMINATED
TO PINS 6 & 7

PINS 6 & 7 ARE GROUNDED
IN ALL RELAYS

REFERENCE TABLE

IC	GND	+5V	V+	V-	N.C.	
U300	8					9
U301	8					9
U302	8	16				
U303	8,13	10,16				
U400			7	4	1	
U401	15.14		13			
U402			7	4		
U500			7	4		
U501			7	4		
U502	7	14				
U503		3		12		
U504		3		12		
U505		3		12		
U506	8	10,16				
U507	3,8		11	6	1,2	
U508			7	4		

A33, A35 Input Ground and Power Chart
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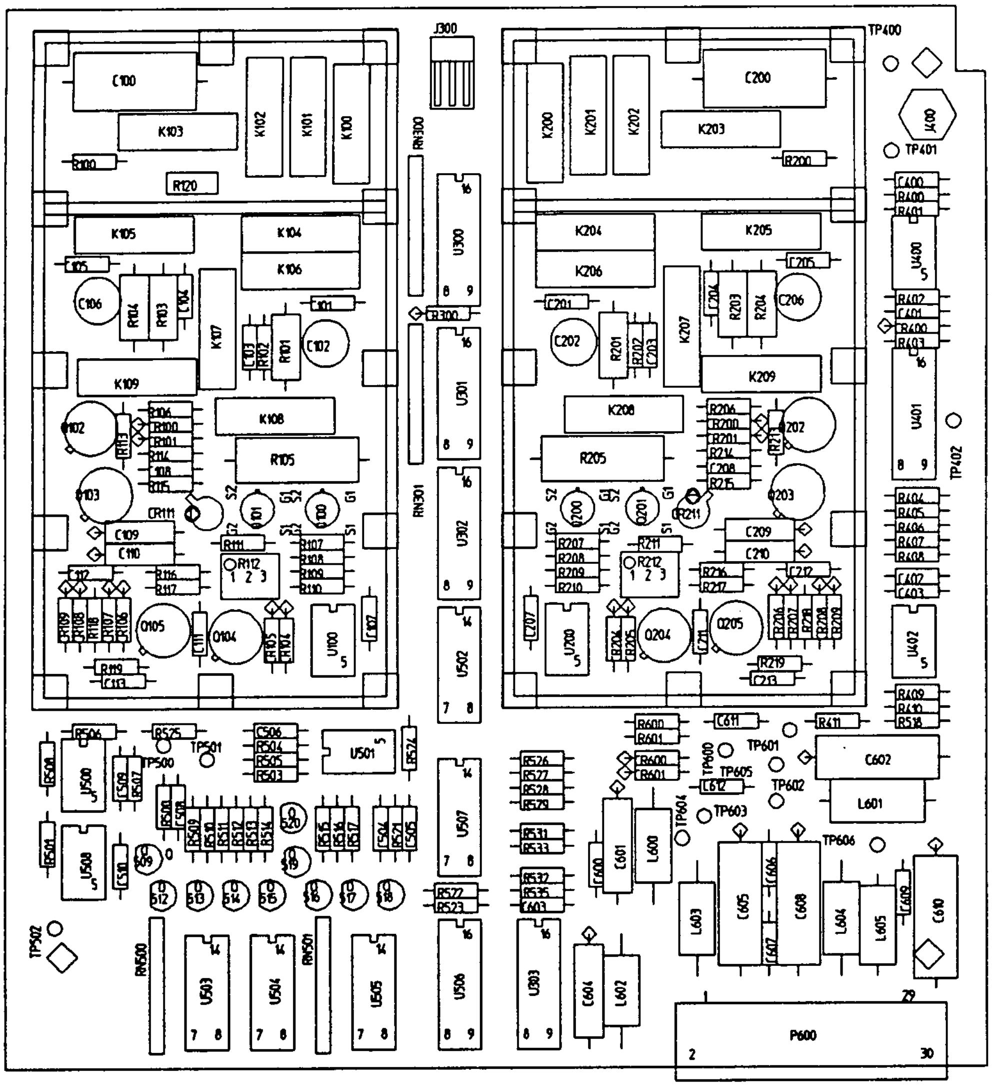

A33, A35 Input Component Locator

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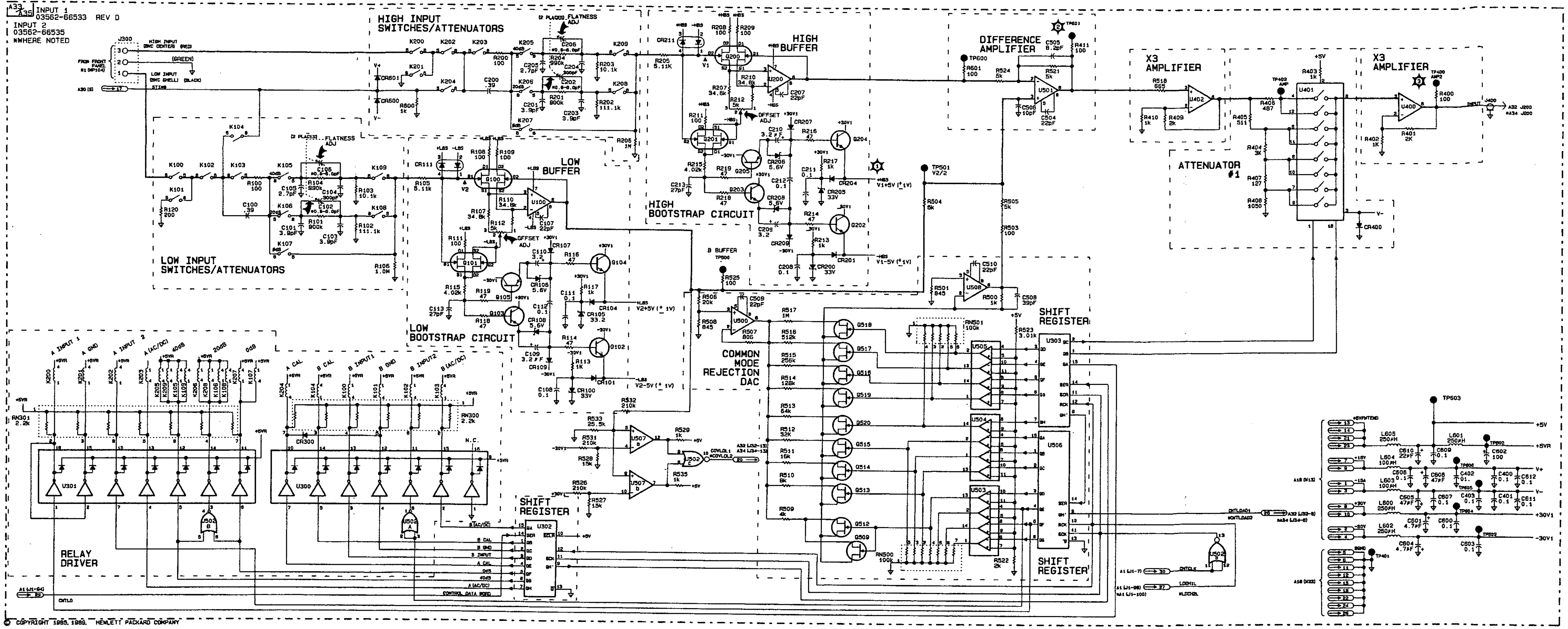

A33, A35 Input Schematic
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HP Digital
Display

HP Digital Display

Introduction

This section contains instructions for troubleshooting and repairing the HP Digital Display. Use this section after performing the adjustment procedures in Section III. This section is used to isolate a failure to the subblock level. Each functional subblock consists of a small number of components, and the technician's expertise is relied upon to isolate the faulty component.

Preventive Maintenance

Painted surfaces can be cleaned with a commercial, spray-type window cleaner or with a mild soap and water solution.

Caution Do not use chemical cleaning agents that might damage the plastics used in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

Corroded spots are best removed with soap and water. Stubborn residue can be removed with a fine abrasive. Protect such areas from further corrosion with an application of silicone resin such as GE DRIFILM 88.

How to Use This Section

Start

Perform the adjustment procedures listed in Section III of this manual. Some apparent malfunctions may be corrected by these adjustments, or failure to obtain a correct adjustment will often reveal the source of the trouble. The procedures are arranged in the recommended sequence of troubleshooting, not in the order of the circuit board assembly number.

Reference

Use the component locators and schematics with each of the troubleshooting procedures.

For the location of cables and boards refer to figure 4-4 in Section IV.

For the circuit block diagrams refer to Section VI.

To understand the display's operation and signal mnemonics refer to Section VI.

Note

After completing a test or repair, check that all jumpers are in the NORMAL or RUN position and that all cables are connected.

Logic Conventions

Positive logic convention is used in this manual unless otherwise noted. Positive logic conventions define a logic "1" or "High" as more positive voltage and a logic "0" or "Low" as the more negative voltage.

Logic Symbols

The logic symbols used in this manual is based on ANSI Y32.14-1973. The purpose of these symbols is to graphically represent device functions so that operation can be understood without having to "look up" how a device works. Basic logic symbols and examples of symbols are shown in figure 8-23. Table 8-61 provides an explanation of function labels used in the schematics.

Waveforms and dc Voltages

Waveforms, dc voltages, and conditions for making these measurements are given on the test pattern illustrations. Since conditions for making measurements may differ from one circuit to another, always check the specific conditions listed for each schematic.

Recommended Test Equipment

The recommended test equipment for troubleshooting is listed in table 1-2. Any item which meets or exceeds the critical requirements can be substituted for the model listed.

Safety Considerations

The HP 3563A is a Safety Class 1 instrument (provided with a protective earth terminal). The instrument and manuals should be reviewed for safety markings and instructions before operation. Refer to the safety symbol table in the preface of this manual.

Warning

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

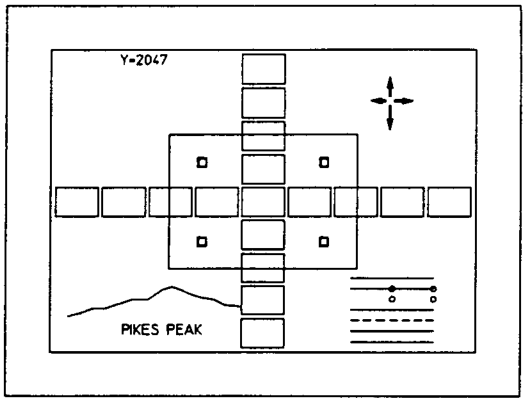
Table 8-60. Assembly Schematic Locator

Order	Assembly	Name
1	—	Block Diagram
2	A82	Vector Processor Control
3	A81	X-Y-Z- Amplifier, Stroke Generator
4	A83	Low Voltage Power Supply
5	A80	High Voltage Power Supply
6	A84	Memory

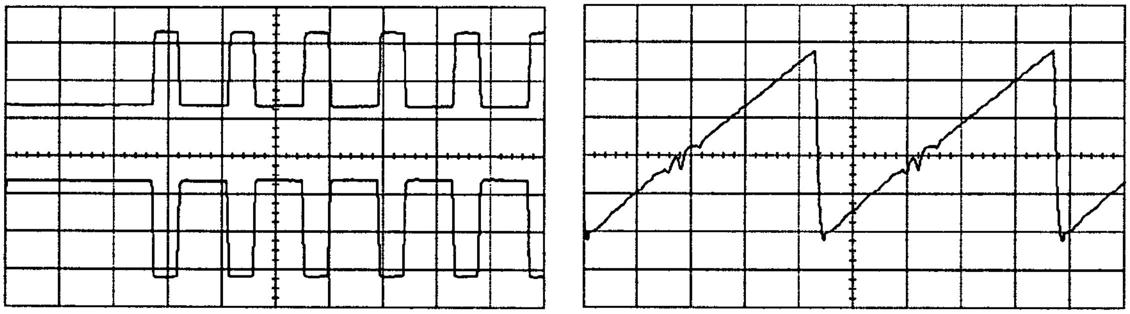
Note

When the A84 Memory Option assembly is installed, jumper packs A82 U3 and A82 U4 must be removed.

HP Digital Display

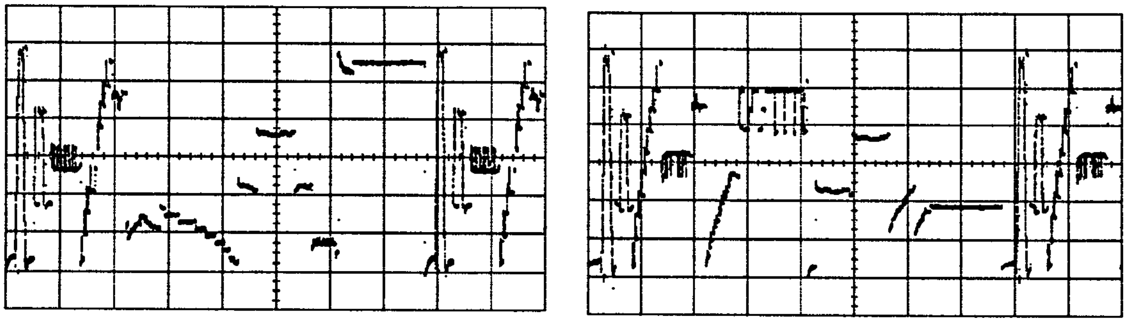


Obtain Primary Test Pattern As Shown Above



Top: LRFD A82, U17 Pin 3
Bottom: LDAV A82, U17 Pin 2V/Div, 50 µs/Div

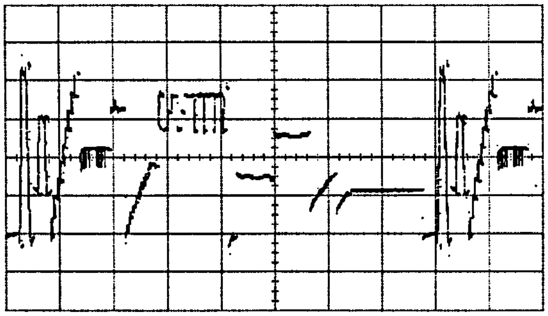
Top: A84, Pin 7
Bottom: A83, Q1 Collector .5 V/Div, 5 µs /Div



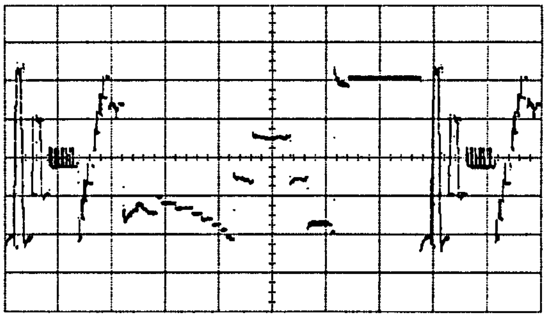
Y DAC Output 200 mV/Div, 2 ms/Div

XDAC Output 200 mV/Div, 2 ms/Div

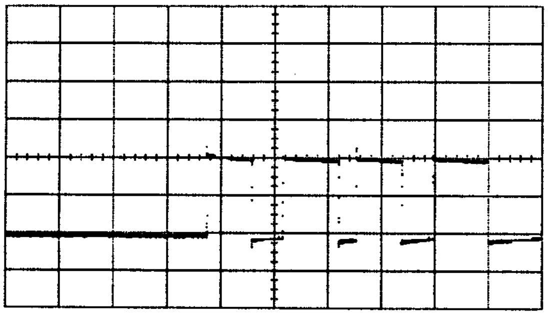
Figure 8-15. HP Digital Display Waveforms



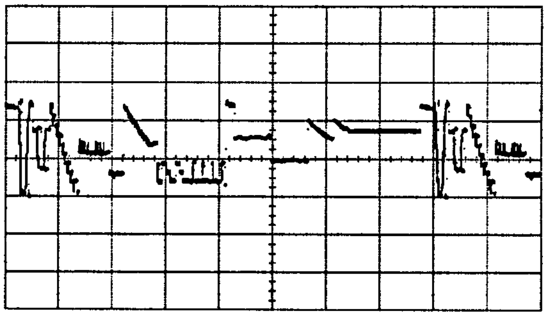
Auxiliary Output at A81 J5 .5 V/Div, 2 ms/Div



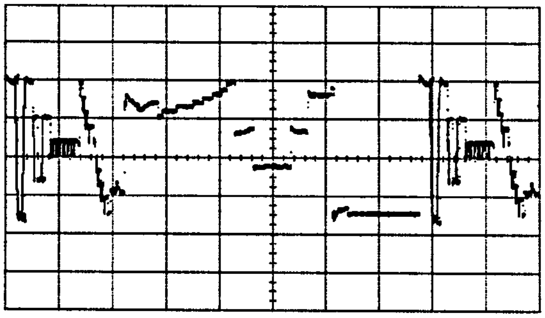
Auuxiliary Y Output at A81 J4 .5 V/Div, 2 ms/Div



Auxiliary Z Output at A81 J3 .5 V/Div, 100 μs/Div



X Output at A81 Q8 Collector
(To Horizontal CRT Deflection Plates) 20 V/Div, 2 ms/Div



Y Output at A81 Q14 Collector
(To Vertical CRT Deflection Plates) 20 V/Div, 2 ms/Div

HP Digital Display Waveforms continued

A82 Vector Processor

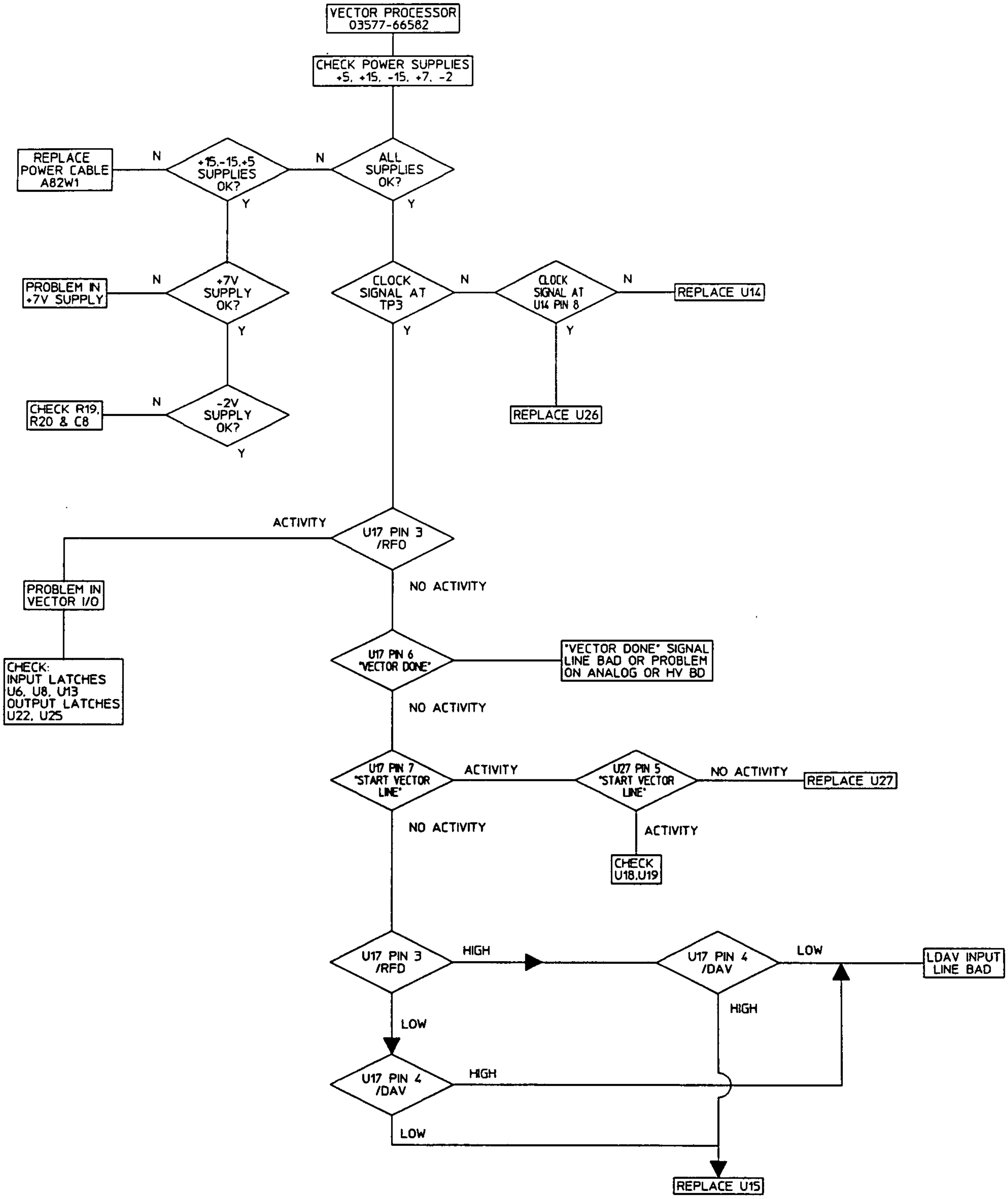


Figure 8-16. A82 Vector Processor Troubleshooting Procedure

A81 X-Y-Z Amplifier/Stroke Generator

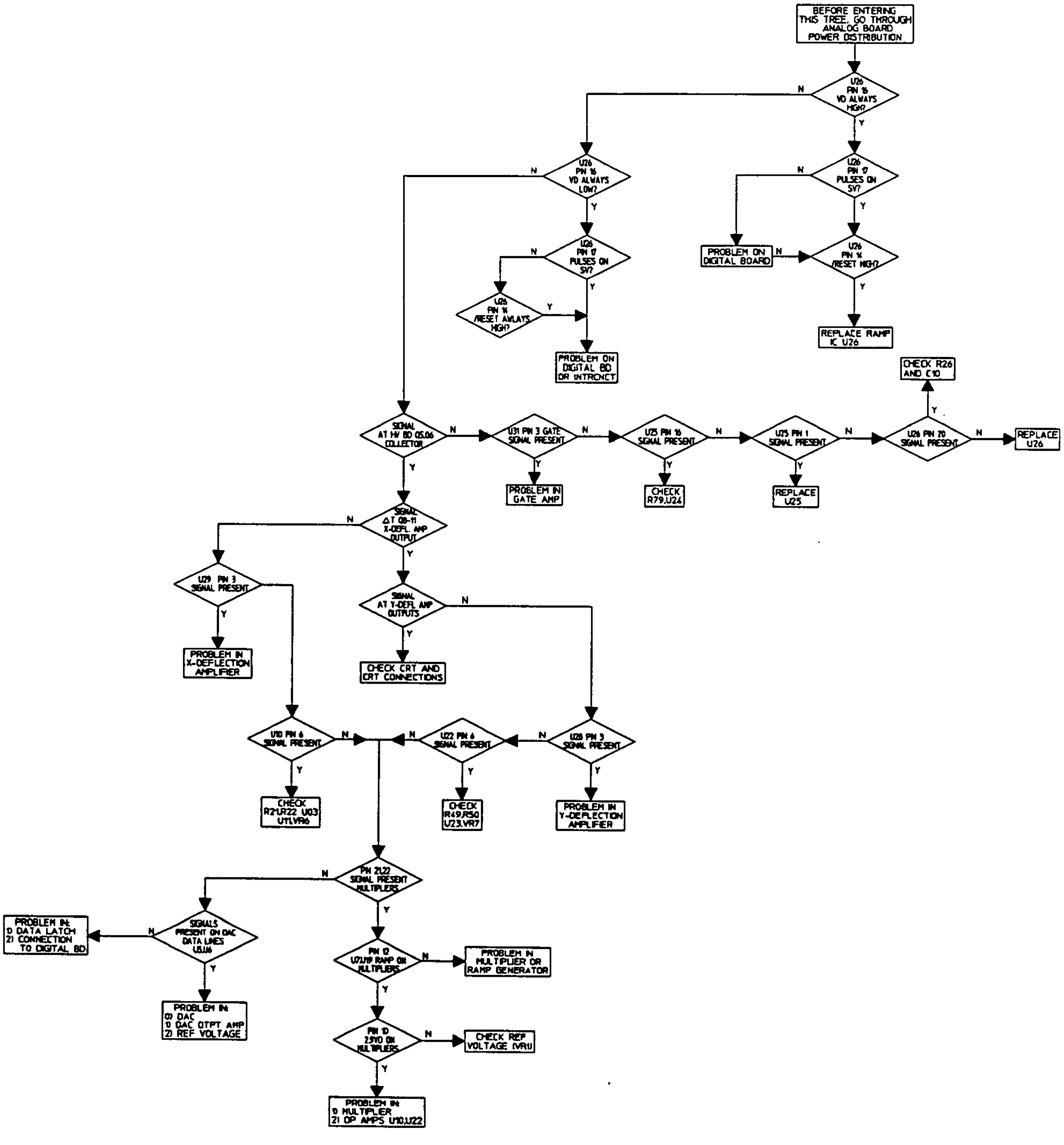
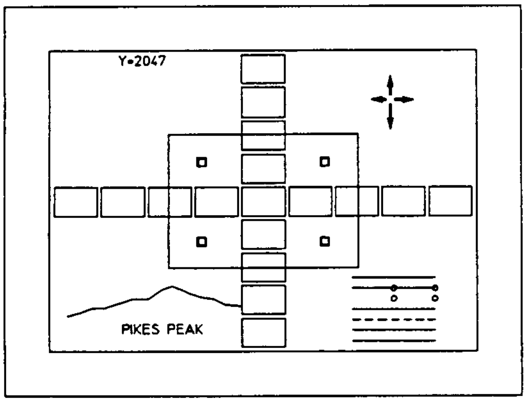
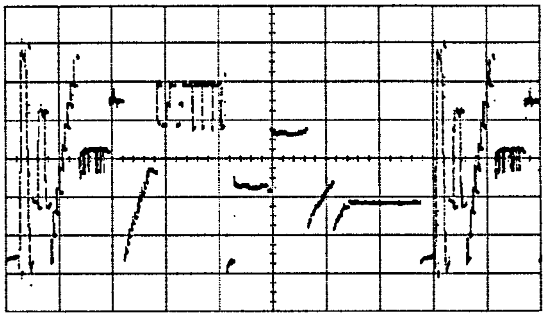

BEFORE ENTERING THIS TREE, GO THROUGH ANALOG BOARD POWER DISTRIBUTION
U26 PIN 16 VD ALWAYS HIGH?
U26 PIN 17 PULSES ON 5V?
PROBLEM ON DIGITAL BOARD
U26 PIN 14 /RESET HIGH?
REPLACE RAMP IC U26
U26 PIN 16 VD ALWAYS LOW?
U26 PIN 17 PULSES ON 5V?
U26 PIN 14 /RESET AWLAYS HIGH?
PROBLEM ON DIGITAL BD OR INTRCNCT
SIGNAL AT HV BD Q5,Q6 COLLECTOR
U31 PIN 3 GATE SIGNAL PRESENT
PROBLEM IN GATE AMP
U25 PIN 16 SIGNAL PRESENT
CHECK R79,U24
U25 PIN 1 SIGNAL PRESENT
REPLACE U25
U26 PIN 20 SIGNAL PRESENT
CHECK R26 AND C10
REPLACE U26
SIGNAL AT Q8-11 X-DEFL AMP OUTPUT
U29 PIN 3 SIGNAL PRESENT
PROBLEM IN X-DEFLECTION AMPLIFIER
SIGNAL AT Y-DEFL AMP OUTPUTS
CHECK CRT AND CRT CONNECTIONS
U10 PIN 6 SIGNAL PRESENT
CHECK R21,R22 U03 U11,VR6
U22 PIN 6 SIGNAL PRESENT
CHECK R49,R50 U23,VR7
U28 PIN 3 SIGNAL PRESENT
PROBLEM IN Y-DEFLECTION AMPLIFIER
PIN 21,22 SIGNAL PRESENT MULTIPLERS
SIGNALS PRESENT ON DAC DATA LINES U5,U6
PROBLEM IN: 1) DATA LATCH 2) CONNECTION TO DIGITAL BD
PROBLEM IN: 0) DAC 1) DAC OTPT AMP 2) REF VOLTAGE
PIN 12 U7,U19 RAMP ON MULTIPLERS
PROBLEM IN MULTIPLIER OR RAMP GENERATOR
PIN 10 2.5VD ON MULTIPLERS
CHECK REF VOLTAGE (VR1)
PROBLEM IN: 1) MULTIPLER 2) OP AMPS U10,U22
Y
N

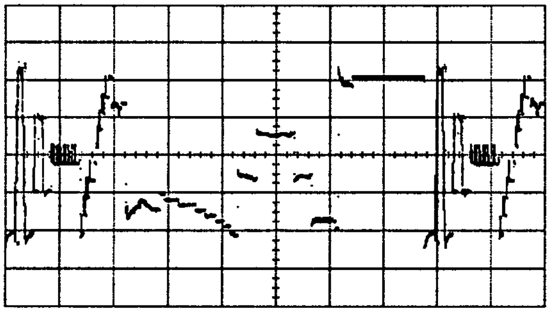
Figure 8-17. A81 X-Y-X Amplifier / Stroke Generator Troubleshooting Procedure



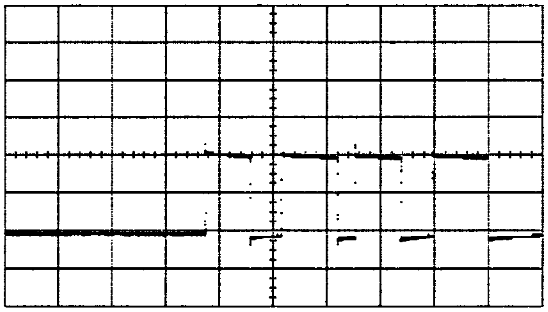
Obtain Primary Test Pattern As Shown Above



Auxiliary X Output at A81 J5 .2 V/Div, 2 ms/Div



Auxiliary Y Output at A81 J4 .5 V/Div, 2 ms/Div



Auxiliary Z Output at A81 J3 .5 V/Div 100 µs/Div

Figure 8-18. A81 X-Y-Z Amplifier / Stroke Generator Waveforms

A83 Low Voltage Power Supply

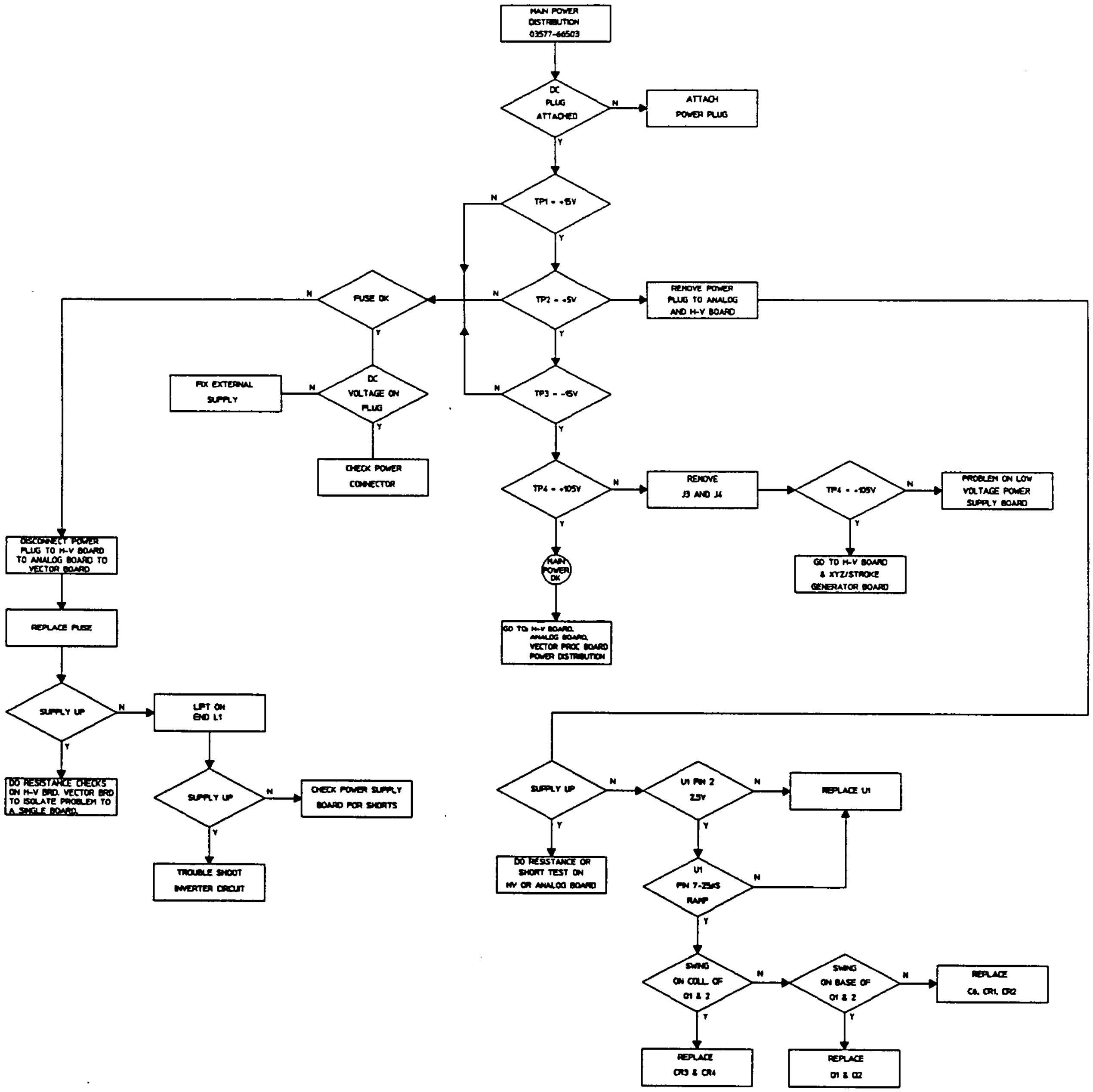
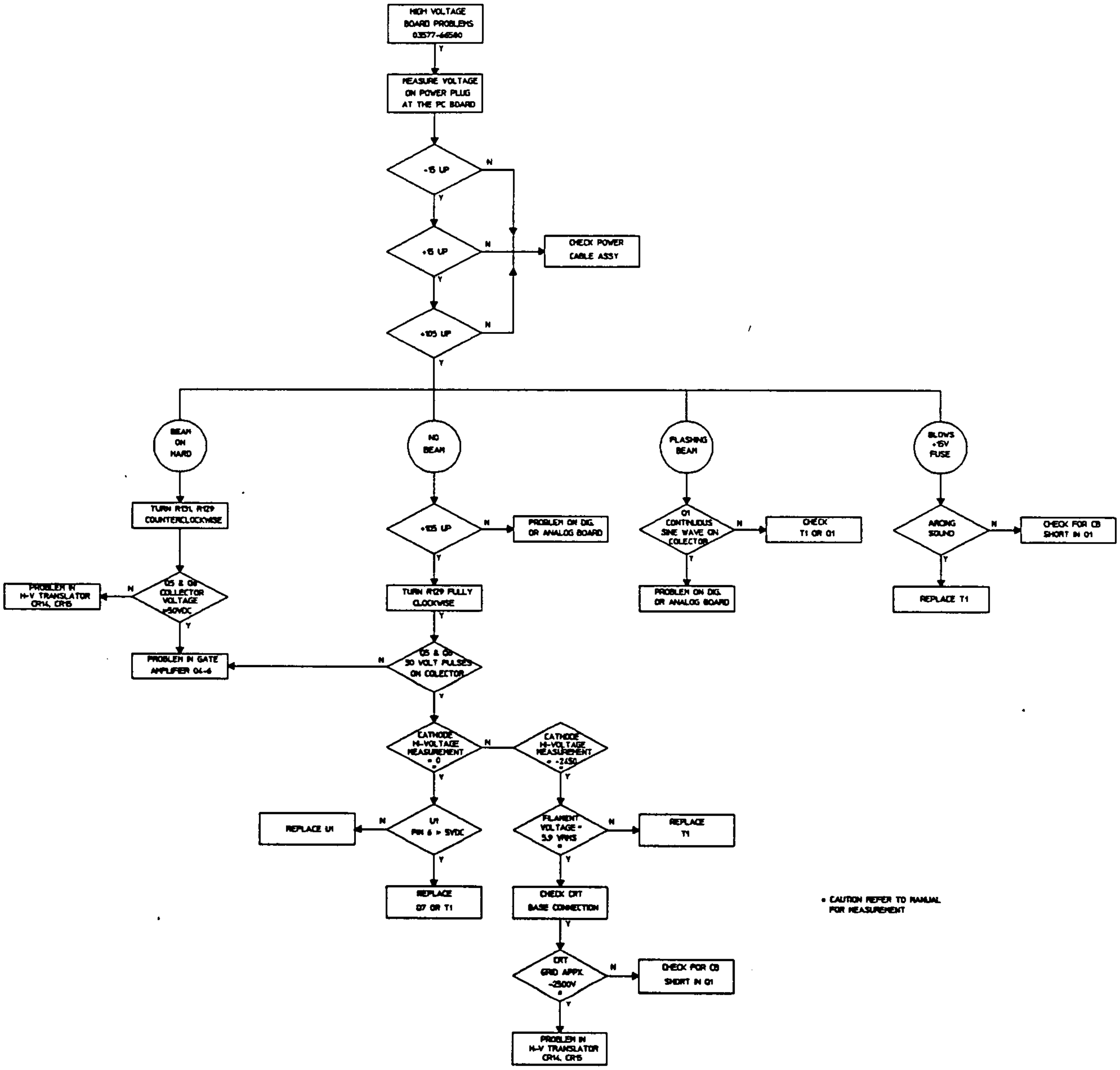

MAIN POWER DISTRIBUTION 03577-66503
DC PLUG ATTACHED
ATTACH POWER PLUG
TP1 = +15V
TP2 = +5V
FUSE OK
REMOVE POWER PLUG TO ANALOG AND H-V BOARD
DC VOLTAGE ON PLUG
FIX EXTERNAL SUPPLY
CHECK POWER CONNECTOR
TP3 = -15V
TP4 = +105V
REMOVE J3 AND J4
TP4 = +105V
PROBLEM ON LOW VOLTAGE POWER SUPPLY BOARD
GO TO H-V BOARD & XYZ/STROKE GENERATOR BOARD
MAIN POWER OK
GO TO: H-V BOARD, ANALOG BOARD, VECTOR PROC BOARD POWER DISTRIBUTION
DISCONNECT POWER PLUG TO H-V BOARD TO ANALOG BOARD TO VECTOR BOARD
REPLACE FUSE
SUPPLY UP
LIFT ON END L1
DO RESISTANCE CHECKS ON H-V BRD. VECTOR BRD TO ISOLATE PROBLEM TO A SINGLE BOARD.
SUPPLY UP
CHECK POWER SUPPLY BOARD FOR SHORTS
TROUBLE SHOOT INVERTER CIRCUIT
SUPPLY UP
U1 PIN 2 2.5V
REPLACE U1
DO RESISTANCE OR SHORT TEST ON HV OR ANALOG BOARD
U1 PIN 7-25μS RAMP
SWING ON COLL. OF Q1 & 2
SWING ON BASE OF Q1 & 2
REPLACE C6, CR1, CR2
REPLACE CR3 & CR4
REPLACE Q1 & Q2
Y
N

Figure 8-19. A83 Low Voltage Power Supply Troubleshooting Procedure

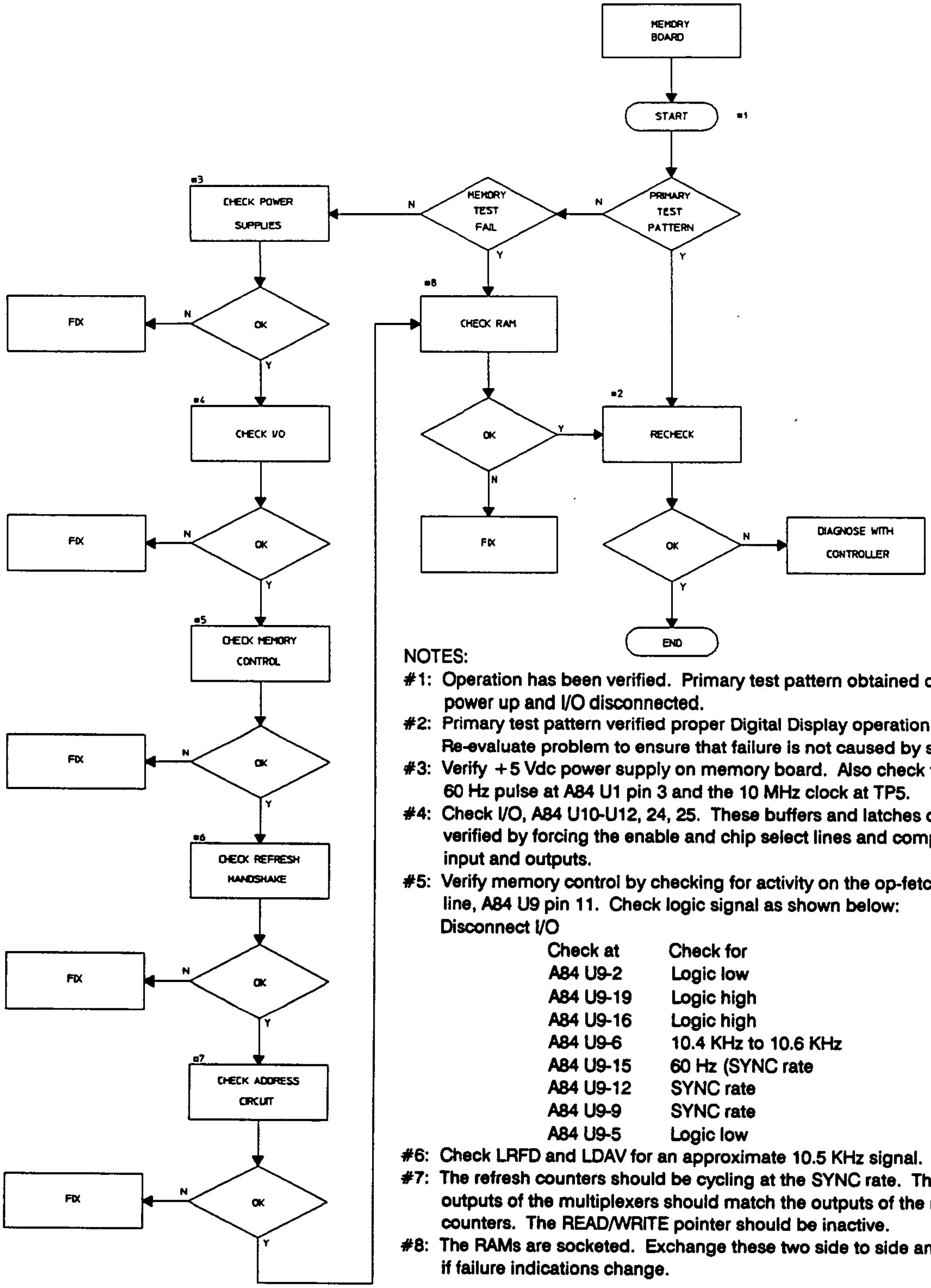
A80 High Voltage Power Supply


HIGH VOLTAGE BOARD PROBLEMS 03577-66580
Y
MEASURE VOLTAGE ON POWER PLUG AT THE PC BOARD
-15 UP
N
Y
+15 UP
N
Y
CHECK POWER CABLE ASSY
+105 UP
N
Y
BEAM ON HARD
NO BEAM
FLASHING BEAM
BLOWS +15V FUSE
TURN R131, R129 COUNTERCLOCKWISE
+105 UP
N
Y
PROBLEM ON DIG. OR ANALOG BOARD
Q1 CONTINUOUS SINE WAVE ON COLECTOR
N
Y
CHECK T1 OR Q1
ARCING SOUND
N
Y
CHECK FOR CB SHORT IN Q1
PROBLEM IN H-V TRANSLATOR CR14, CR15
N
Q5 & Q8 COLLECTOR VOLTAGE +50VDC
Y
TURN R129 FULLY CLOCKWISE
PROBLEM ON DIG. OR ANALOG BOARD
REPLACE T1
PROBLEM IN GATE AMPLIFIER Q4-6
N
Q5 & Q8 30 VOLT PULSES ON COLECTOR
Y
CATHODE HI-VOLTAGE MEASUREMENT = 0 *
N
Y
CATHODE HI-VOLTAGE MEASUREMENT = -2450 *
Y
REPLACE U1
N
U1 PIN 6 > 5VDC
Y
FILAMENT VOLTAGE = 5.9 VRMS *
N
Y
REPLACE T1
REPLACE Q7 OR T1
CHECK CRT BASE CONNECTION
Y
CRT GRID APPX. -2500V *
N
Y
CHECK FOR CB SHORT IN Q1
PROBLEM IN H-V TRANSLATOR CR14, CR15

* CAUTION REFER TO MANUAL FOR MEASUREMENT

Figure 8-20. A80 High Voltage Power Supply Troubleshooting Procedure

A84 Memory



NOTES:

#1: Operation has been verified. Primary test pattern obtained during power up and I/O disconnected.

#2: Primary test pattern verified proper Digital Display operation. Re-evaluate problem to ensure that failure is not caused by system.

#3: Verify +5 Vdc power supply on memory board. Also check for the 60 Hz pulse at A84 U1 pin 3 and the 10 MHz clock at TP5.

#4: Check I/O, A84 U10-U12, 24, 25. These buffers and latches can be verified by forcing the enable and chip select lines and comparing input and outputs.

#5: Verify memory control by checking for activity on the op-fetch line, A84 U9 pin 11. Check logic signal as shown below:
Disconnect I/O

Check at	Check for
A84 U9-2	Logic low
A84 U9-19	Logic high
A84 U9-16	Logic high
A84 U9-6	10.4 KHz to 10.6 KHz
A84 U9-15	60 Hz (SYNC rate
A84 U9-12	SYNC rate
A84 U9-9	SYNC rate
A84 U9-5	Logic low

#6: Check LRFD and LDAV for an approximate 10.5 KHz signal.

#7: The refresh counters should be cycling at the SYNC rate. The outputs of the multiplexers should match the outputs of the refresh counters. The READ/WRITE pointer should be inactive.

#8: The RAMs are socketed. Exchange these two side to side and note if failure indications change.

Figure 8-21. A84 Memory Circuit Troubleshooting Procedure

Symbols and Labels

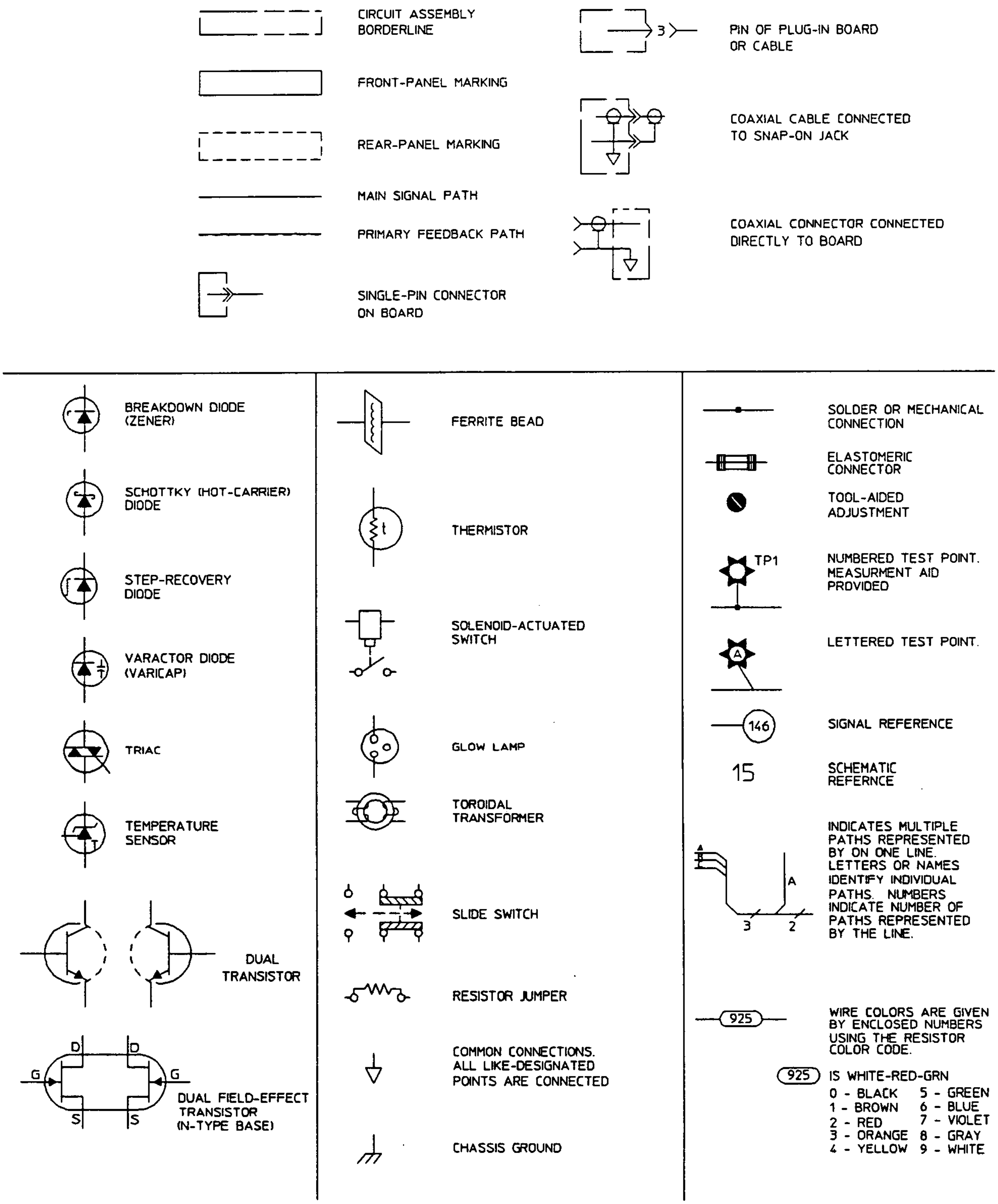

CIRCUIT ASSEMBLY BORDERLINE
FRONT-PANEL MARKING
REAR-PANEL MARKING
MAIN SIGNAL PATH
PRIMARY FEEDBACK PATH
SINGLE-PIN CONNECTOR ON BOARD
3
PIN OF PLUG-IN BOARD OR CABLE
COAXIAL CABLE CONNECTED TO SNAP-ON JACK
COAXIAL CONNECTOR CONNECTED DIRECTLY TO BOARD
BREAKDOWN DIODE (ZENER)
SCHOTTKY (HOT-CARRIER) DIODE
STEP-RECOVERY DIODE
VARACTOR DIODE (VARICAP)
TRIAC
TEMPERATURE SENSOR
T
DUAL TRANSISTOR
D
D
G
G
S
S
DUAL FIELD-EFFECT TRANSISTOR (N-TYPE BASE)
FERRITE BEAD
t
THERMISTOR
SOLENOID-ACTUATED SWITCH
GLOW LAMP
TOROIDAL TRANSFORMER
SLIDE SWITCH
RESISTOR JUMPER
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED
CHASSIS GROUND
SOLDER OR MECHANICAL CONNECTION
ELASTOMERIC CONNECTOR
TOOL-AIDED ADJUSTMENT
TP1
NUMBERED TEST POINT. MEASURMENT AID PROVIDED
A
LETTERED TEST POINT.
146
SIGNAL REFERENCE
15
SCHEMATIC REFERNCE
A
3
2
INDICATES MULTIPLE PATHS REPRESENTED BY ON ONE LINE. LETTERS OR NAMES IDENTIFY INDIVIDUAL PATHS. NUMBERS INDICATE NUMBER OF PATHS REPRESENTED BY THE LINE.
925
WIRE COLORS ARE GIVEN BY ENCLOSED NUMBERS USING THE RESISTOR COLOR CODE.
925 IS WHITE-RED-GRN
0 - BLACK
1 - BROWN
2 - RED
3 - ORANGE
4 - YELLOW
5 - GREEN
6 - BLUE
7 - VIOLET
8 - GRAY
9 - WHITE

Figure 8-22. Schematic Diagram Symbols

Table 8-61. Function Labels

▷	AMPLIFIER/BUFFER
1 ⎍	MONOSTABLE MULTIVIBRATOR (ONE-SHOT)
&	AND GATE
≧ 1	OR GATE
= 1	EXCLUSIVE OR GATE
X—Y	ENCODER, DECODER
XMAX—Y	PRIORITY ENCODER
CNTR	COUNTER
DEMUX	DEMULTIPLEXER
FF	FLIP-FLOP
RAM	RANDOM-ACCESS MEMORY
REG	REGESTER
ROM	READ-ONLY MEMORY
SAR	SUCCESSIVE APPROXIMATION REGESTER
SEL	SELECTER
SREG	SHIFT REGESTER
TX/RX	TRANSMITTER/RECEIVER

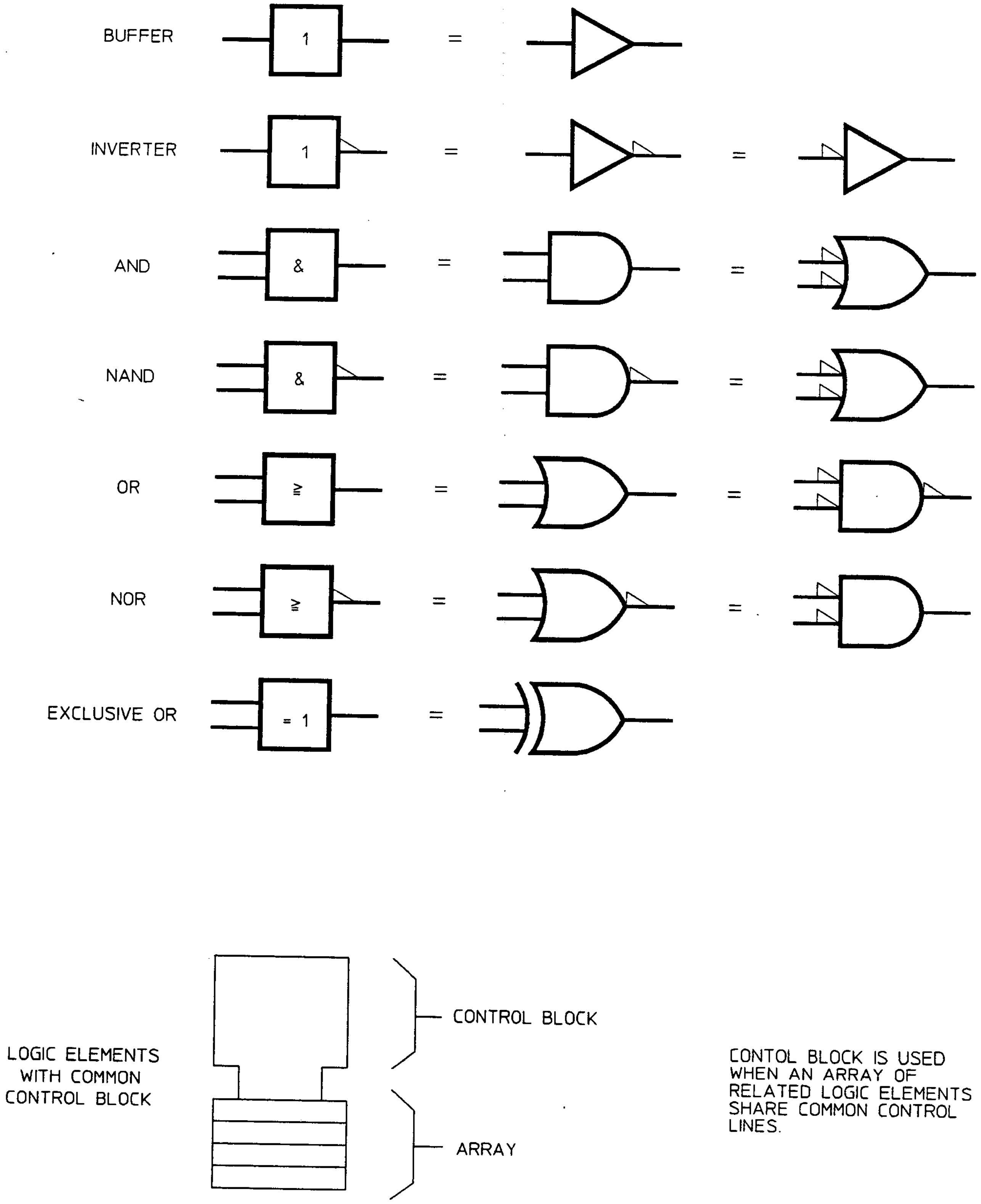
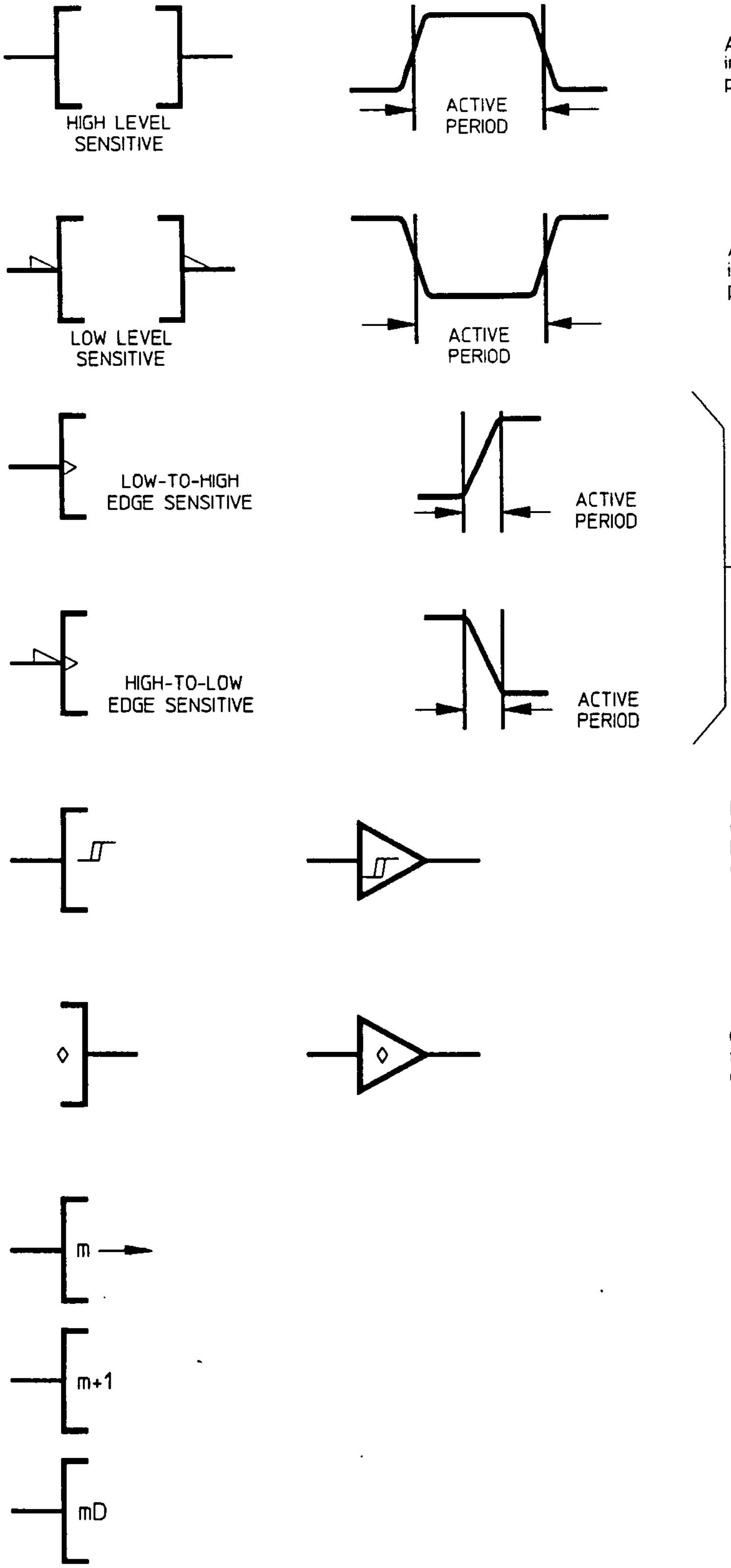


Figure 8-23. Basic Logic Symbols



ACTIVE HIGH inputs and outputs - indicated by the absence of the polarity indicator (◺).

ACTIVE LOW inputs and outputs - indicated by the presence of the polarity indicator (◺).

EDGE SENSITVE (Dynamic) inputs - indicated by the presence of the dynamic indicator symbol (>).

BI-THRESHOLD (Hysteresis) input (⎍) - input takes on internal high state when external signal exceeds high threshold value. State is maintained until external signal falls below a lower threshold value

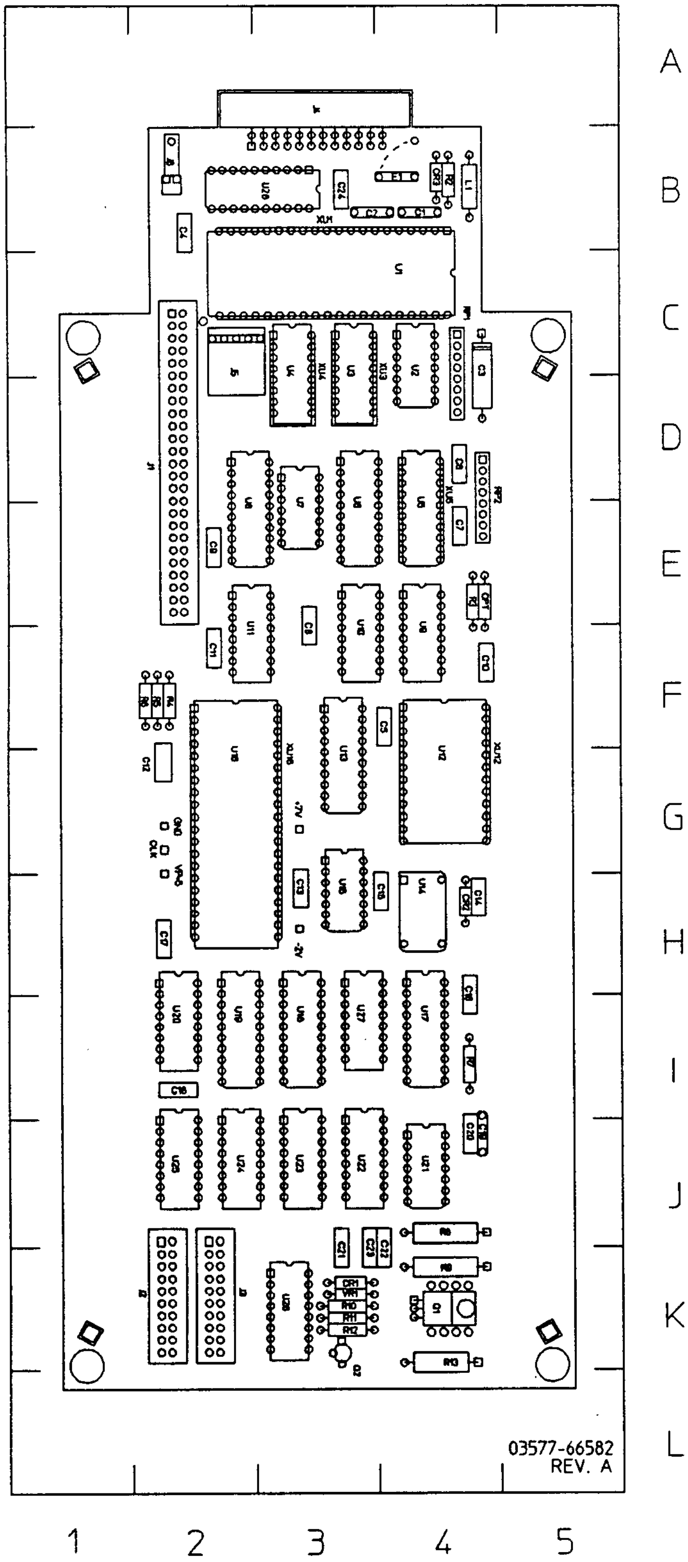
OPEN COLLECTOR output (◊) - forms a part of a distributed connector.

SHIFT RIGHT (Down) input of register. m may be other qualifiers or dependency notation.

COUNT UP input of a counter. m may be other qualifiers or dependency notation.

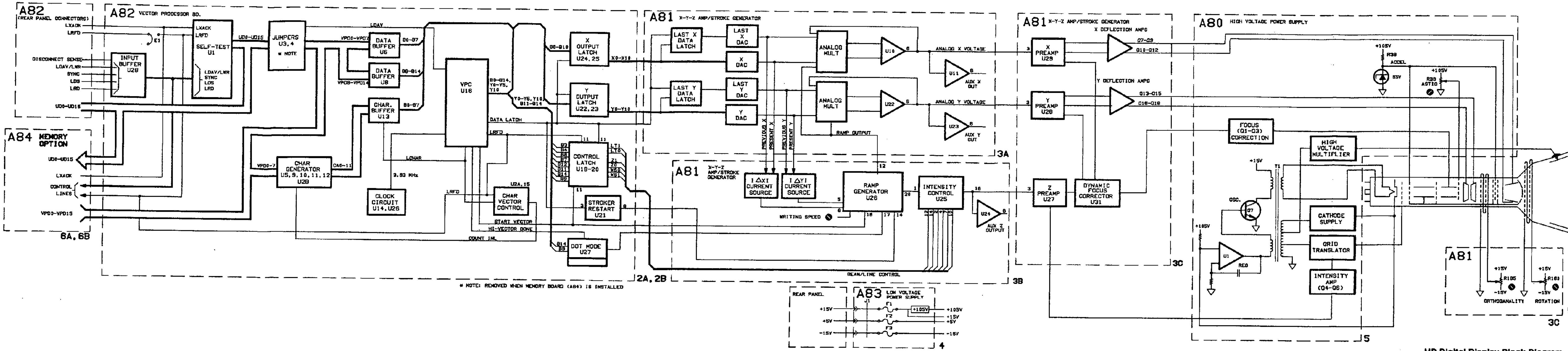
DATA input. m may be other qualifiers or dependency notation.

Figure 8-24. Qualifying Symbols



Ref Desig	Grid Loc	Ref Desig	Grid Loc
C1	B-4	R8	J-4
C2	B-3	R9	K-4
C3	C-4	R10	K-3
C4	C-2	R11	K-3
C5	G-3	R12	K-3
C6	E-4	R13	K-4
C7	E-4	RP1	C-4
C8	F-3	RP2	D-4
C9	E-2	TP1	G-2
C10	F-4	TP2	G-2
C11	F-2	TP3	H-2
C12	G-2	TP4	G-3
C13	H-3	TP5	H-3
C14	H-4	U1	B-4
C15	H-3	U2	C-4
C16	I-4	U3	C-3
C17	H-2	U4	C-3
C18	I-2	U5	D-4
C19	J-4	U6	D-3
C20	J-4	U7	D-3
C21	K-3	U8	D-2
C22	K-3	U9	E-4
C23	K-3	U10	E-3
C24	B-3	U11	E-2
CR1	K-3	U12	F-4
CR2	H-4	U13	F-3
CR3	B-4	U14	H-4
E1	B-4	U15	H-3
J1	C-2	U16	F-2
J2	K-2	U17	I-4
J3	K-2	U18	I-3
J4	B-2	U19	I-2
J5	C-2	U20	I-2
J6	B-2	U21	J-4
L1	B-4	U22	J-3
Q1	K-4	U23	J-3
Q2	K-3	U24	J-2
R2	B-4	U25	J-2
R3	F-4	U26	K-2
R4	F-2	U27	I-3
R5	F-2	U28	B-3

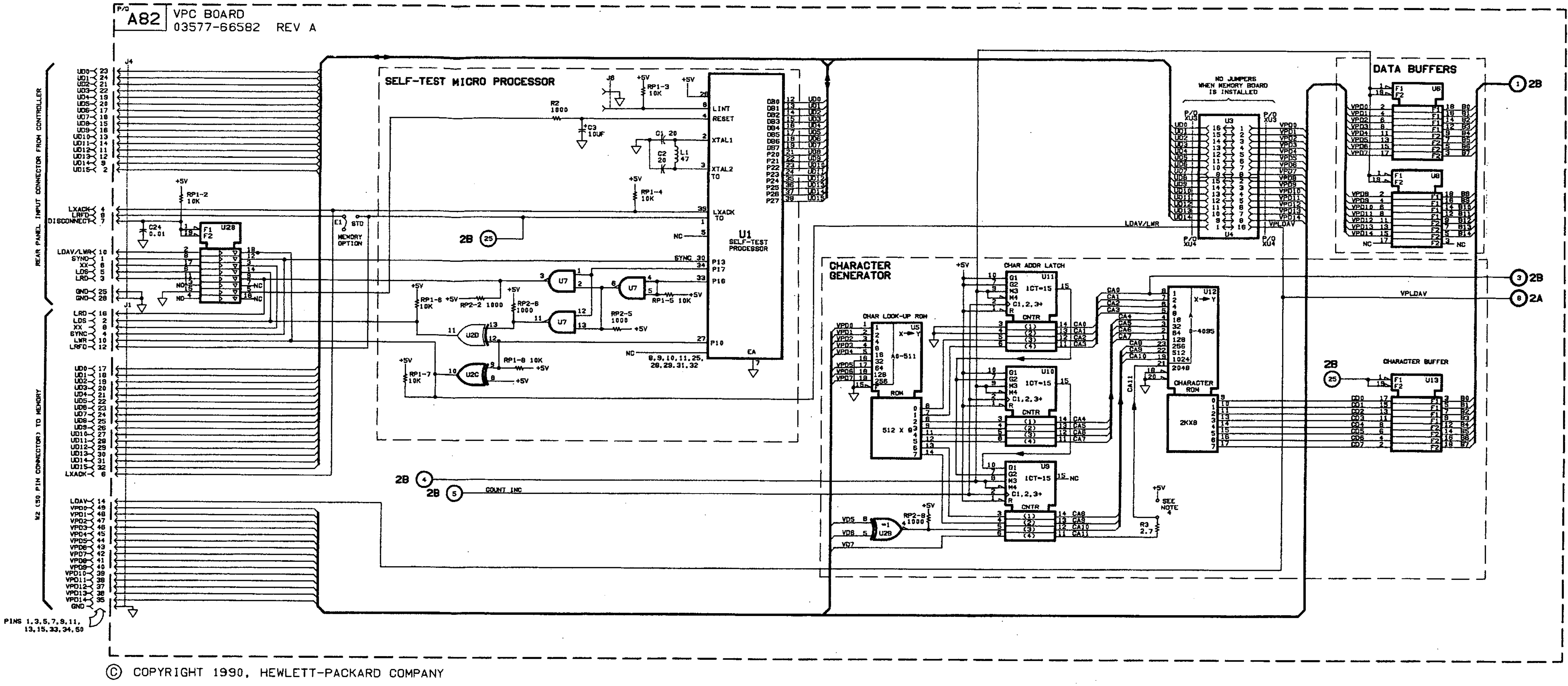
A82 Vector Processor Component Locator
P/N 03577-66582 Rev A
Page 1 of 3



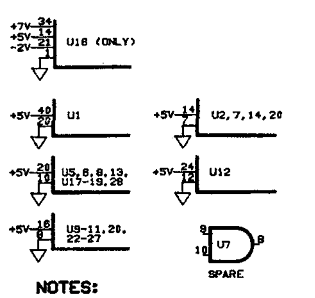
SERVICE SHEET 1

BLOCK DIAGRAM

HP Digital Display Block Diagram
P/N 03562-60150
Page 1 of 1


P/O A82 VPC BOARD 03577-66582 REV A
SELF-TEST MICRO PROCESSOR
U1 SELF-TEST PROCESSOR
CHARACTER GENERATOR
CHAR LOOK-UP ROM
CHAR ADDR LATCH
CHARACTER ROM 2KX8
DATA BUFFERS
CHARACTER BUFFER
NO JUMPERS WHEN MEMORY BOARD IS INSTALLED
MEMORY OPTION
REAR PANEL INPUT CONNECTOR FROM CONTROLLER
W2 (50 PIN CONNECTOR) TO MEMORY
PINS 1,3,5,7,9,11, 13,15,33,34,50
LDAV/LWR
VPLDAV
COUNT INC
2B
2A

IC DEVICE POWER CONNECTIONS



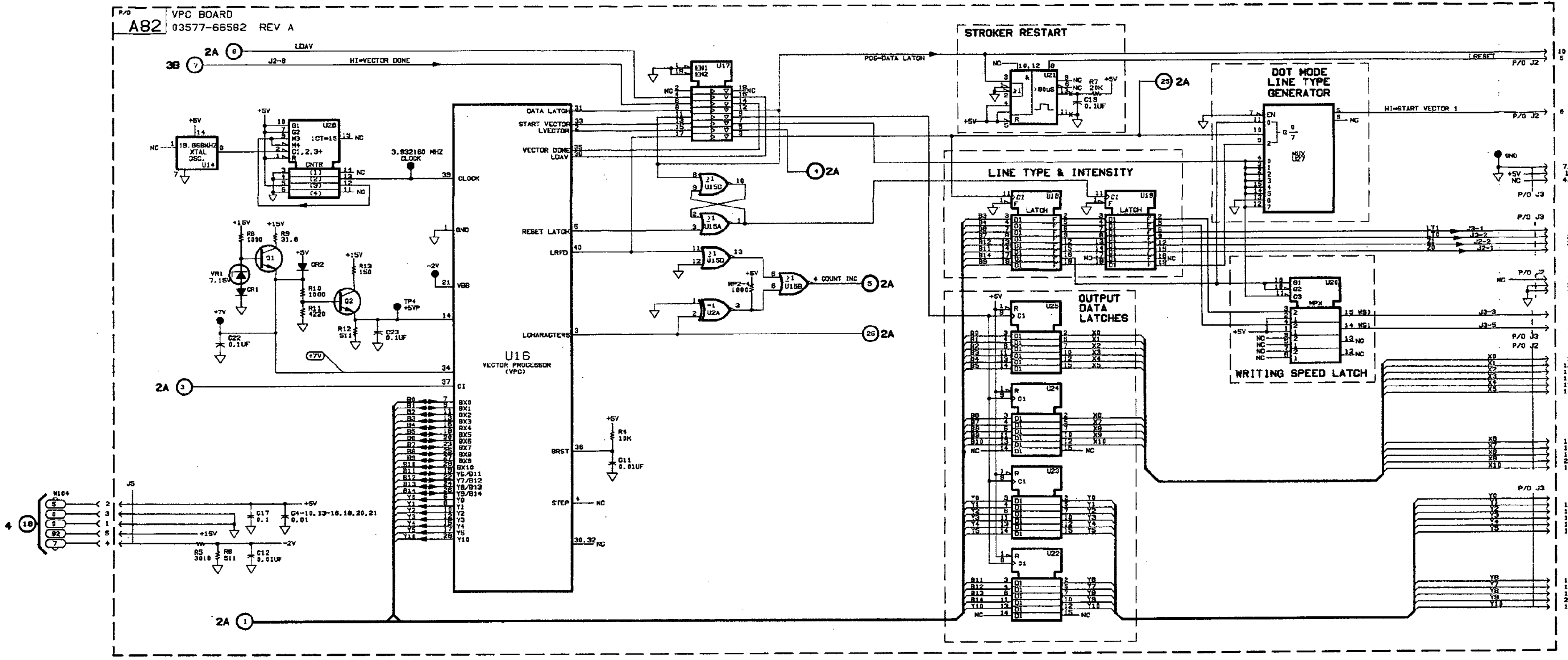
NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. R3 SHOWN IN POSITION FOR 32K ROM. USE ALTERNATE POSITION FOR 16K ROM.
5. WHEN MEMORY IS INSTALLED, JUMPERS U3 & U4 MUST BE REMOVED.
6. JUMPER E1 SHOWN "MEMORY INSTALLED". ALTERNATE POSITION IS FOR NO MEMORY.

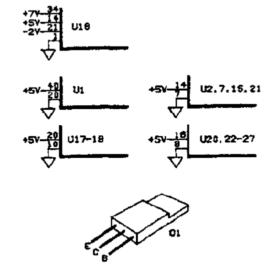
PARTS ON THIS SCHEMATIC
C1-3,24 E1 J1,4,6 R2,3 RP1,2 U1-8,10-13,28

SERVICE SHEET **2A**
P/O VECTOR PROCESSOR (A82)

A82 Vector Processor Schematic
P/N 03577-66582
Page 2 of 3



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   - RESISTANCE IN OHMS
   - CAPACITANCE IN PICOFARADS
   - INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   - LOGIC LEVELS ARE TTL:
     - +2.0V TO +5.0V=LOGIC"1"=H
     - 0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC	
A82	CHASSIS
C4-23 CR1,2 J2,3,5 Q1,2 R4-13 U14-27 VR1	W100 W101 W104

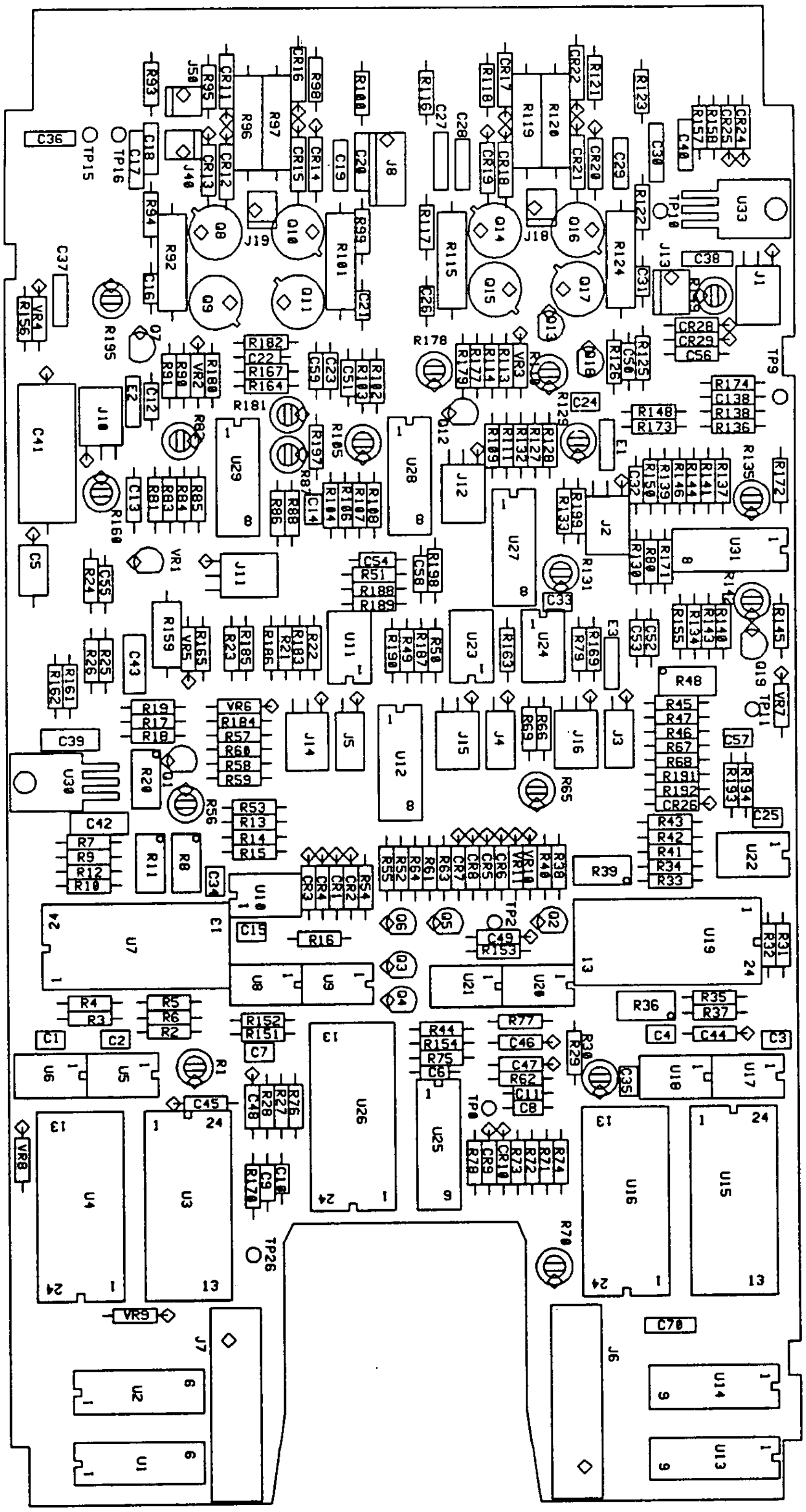
SERVICE SHEET 2B

P/O VECTOR PROCESSOR (A82)

A82 Vector Processor Schematic
P/N 03577-66582
Page 3 of 3

Ref Desig	Grid Loc	Ref Desig	Grid Loc	Ref Desig	Grid Loc	Ref Desig	Grid Loc	Ref Desig	Grid Loc	Ref Desig	Grid Loc	Ref Desig	Grid Loc
C1	I-1	C55	E-2	J20	H-3	R31	G-6	R83	D-2	R137	D-6	R191	F-6
C2	J-2	C56	C-6	J21	I-3	R32	G-6	R84	D-2	R138	E-6	R192	F-6
C3	H-6	C57	F-6	J22	C-2	R33	G-6	R85	D-2	R139	D-6	R193	F-6
C4	H-6	C58	E-4	Q1	F-2	R34	G-6	R86	D-3	R140	E-6	R194	F-6
C5	E-1	C59	C-3	Q2	G-5	R35	H-6	R87	D-3	R141	D-6	R195	C-2
C6	H-4	CR1	G-3	Q3	G-4	R36	H-5	R88	D-3	R142	E-6	TP2	G-4
C7	H-3	CR2	G-3	Q4	H-4	R37	H-6	R90	C-2	R143	E-6	TP9	D-6
C8	I-4	CR3	G-3	Q5	G-4	R38	G-5	R91	C-2	R144	D-6	TP10	B-6
C9	I-3	CR4	G-3	Q6	G-4	R39	G-5	R92	B-2	R145	D-6	TP11	F-6
C10	I-3	CR5	G-4	Q7	C-2	R40	G-5	R93	A-2	R146	D-6	U1	K-1
C11	I-4	CR6	G-4	Q8	C-2	R41	G-6	R94	B-2	R147	D-6	U2	K-1
C12	D-2	CR7	G-4	Q9	C-3	R42	G-6	R95	A-2	R148	D-6	U3	I-2
C13	D-2	CR8	G-4	Q10	C-3	R43	G-6	R96	A-3	R149	C-6	U4	J-2
C14	D-3	CR9	I-4	Q11	C-3	R44	H-4	R97	A-3	R150	D-5	U5	H-2
C16	C-2	CR10	I-4	Q12	D-4	R45	F-6	R98	A-3	R151	H-3	U6	H-1
C17	B-2	CR11	B-2	Q13	C-5	R46	F-6	R99	B-3	R152	H-3	U7	H-1
C18	B-2	CR12	B-2	Q14	C-4	R47	F-6	R100	A-3	R153	G-5	U8	H-3
C19	B-3	CR13	B-2	Q15	C-4	R48	F-6	R101	B-3	R154	H-4	U9	H-3
C20	B-3	CR14	B-3	Q16	C-5	R49	E-4	R102	C-4	R155	E-6	U10	G-3
C21	C-3	CR15	B-3	Q17	C-5	R50	E-4	R103	C-3	R156	C-1	U11	F-3
C22	C-3	CR16	B-3	Q18	C-5	R51	E-4	R104	D-3	R157	B-6	U12	F-4
C23	C-3	CR17	B-4	Q19	F-6	R52	G-4	R105	D-3	R158	B-6	U13	K-6
C24	D-5	CR18	B-4	R1	H-2	R53	G-3	R106	D-3	R159	E-2	U14	J-6
C26	C-4	CR19	B-4	R2	H-2	R54	G-3	R107	D-3	R160	D-2	U15	I-6
C27	B-4	CR20	B-5	R3	H-1	R55	G-4	R108	D-4	R161	E-1	U16	J-6
C28	B-4	CR21	B-5	R4	G-1	R56	F-2	R109	D-4	R162	E-1	U17	H-6
C29	B-5	CR22	B-5	R5	H-2	R57	F-3	R110	D-5	R163	E-4	U18	H-6
C30	B-6	CR23	D-6	R6	H-2	R58	F-3	R111	D-4	R164	D-3	U19	G-6
C31	C-5	CR24	B-6	R7	G-2	R59	F-3	R113	C-4	R165	E-2	U20	H-5
C32	D-5	CR25	B-6	R8	G-2	R60	F-3	R114	C-4	R167	D-3	U21	H-4
C33	D-5	CR26	G-6	R9	G-2	R61	G-4	R115	B-4	R169	E-5	U22	G-6
C34	G-2	E1	D-5	R10	G-2	R62	H-5	R116	A-4	R170	I-3	U23	F-4
C35	H-5	E2	E-1	R11	G-1	R63	G-4	R117	B-4	R171	E-6	U24	E-5
C36	B-1	E3	E-5	R12	G-2	R64	G-4	R118	A-4	R172	D-6	U25	I-4
C37	C-1	J1	C-6	R13	G-3	R65	G-5	R119	A-5	R173	D-5	U26	I-4
C38	C-6	J2	D-5	R14	G-3	R66	F-5	R120	A-5	R174	D-5	U27	D-4
C39	F-1	J3	F-5	R15	G-3	R67	F-6	R121	A-5	R175	C-6	U28	D-4
C40	B-6	J4	F-4	R16	G-3	R68	F-6	R122	B-5	R176	C-6	U29	D-2
C41	D-1	J5	F-3	R17	F-2	R69	F-5	R123	A-5	R177	C-4	U30	F-2
C42	G-2	J6	K-5	R18	F-2	R70	J-5	R124	B-5	R178	D-4	U31	E-6
C43	E-2	J7	J-2	R19	F-2	R71	I-5	R125	C-5	R179	C-4	U33	C-6
C44	H-6	J8	B-4	R20	F-2	R72	I-5	R126	C-5	R180	C-2	VR1	E-2
C45	I-2	J9	B-2	R21	E-3	R73	I-5	R127	D-5	R181	D-3	VR2	C-2
C46	H-5	J10	D-2	R22	E-3	R74	I-5	R128	D-5	R182	C-3	VR3	C-5
C47	H-5	J11	E-2	R23	E-3	R75	H-4	R129	D-5	R183	E-3	VR4	C-1
C48	H-2	J12	D-4	R24	E-2	R76	H-3	R130	E-5	R184	F-3	VR5	F-2
C49	H-6	J13	C-6	R25	E-2	R77	H-5	R131	E-5	R185	E-3	VR6	F-3
C50	C-5	J14	F-3	R26	E-2	R78	I-4	R132	D-5	R186	E-3	VR7	F-6
C51	C-3	J15	F-4	R27	H-3	R79	E-5	R133	D-5	R187	E-4	VR8	H-2

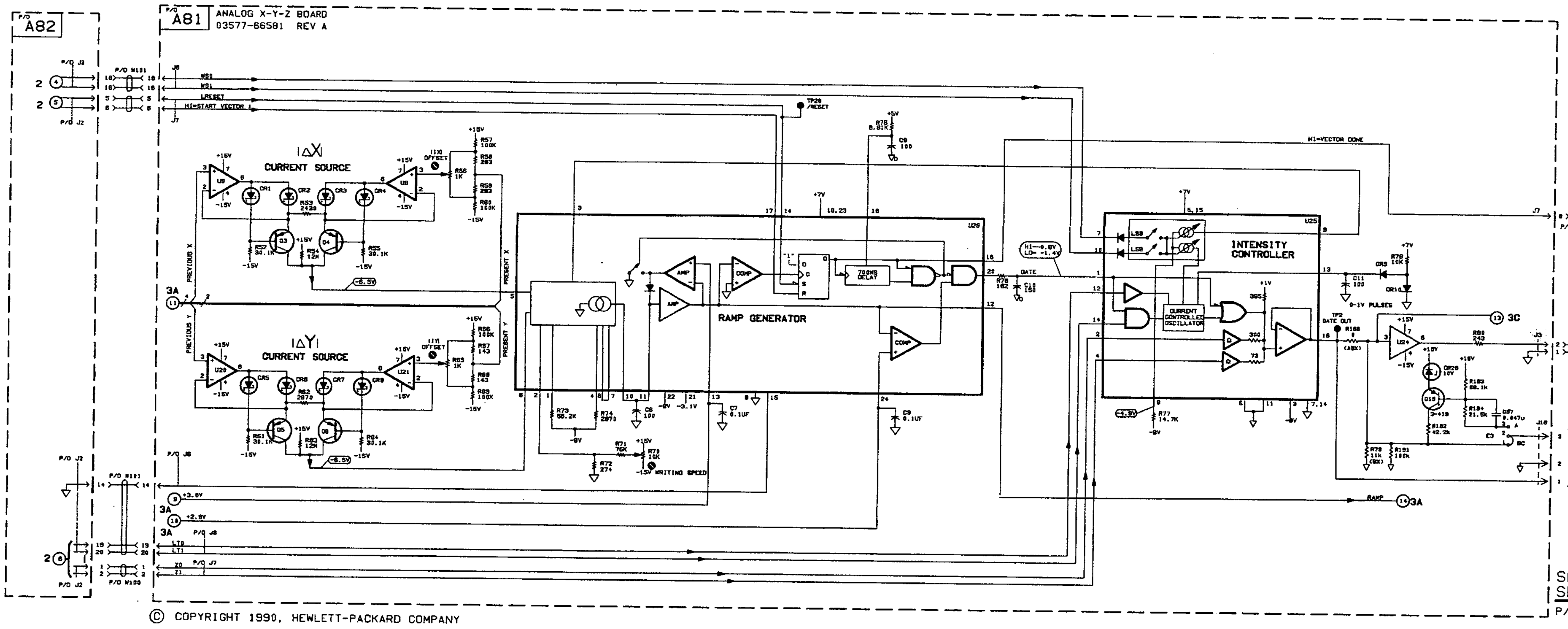
A81 X-Y-Z Amplifier/Stroke Generator Reference Designators
P/N 03577-66581
Page 1 of 5

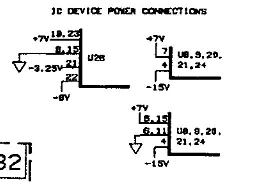


A81 X-Y-Z Amplifier/Stroke Generator Component Locator

P/N 03577-66581 Rev A

Page 2 of 5





NOTES:
1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2V TO +5V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC	
P/O A81	CHASSIS
C6-11,57 CR1-11,28 E3 J3,6,7 Q3-6,19 R52-88,181-184 U8,9,20,21,24-26	P/O W100 P/O W101

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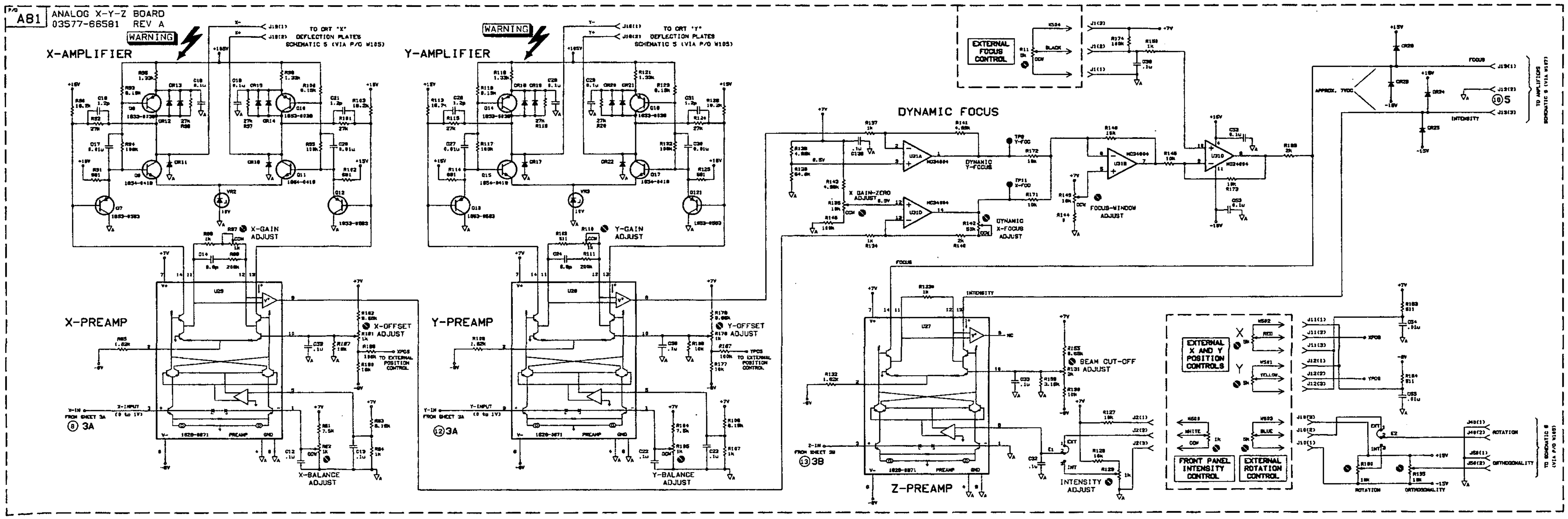
SERVICE SHEET 3B

P/O X-Y-Z AMP/STROKE GENERATOR (A81)

A81 X-Y-Z Amplifier/Stroke Generator Schematic
P/N 03577-66581
Page 4 of 5



PARTS ON THIS SCHEMATIC

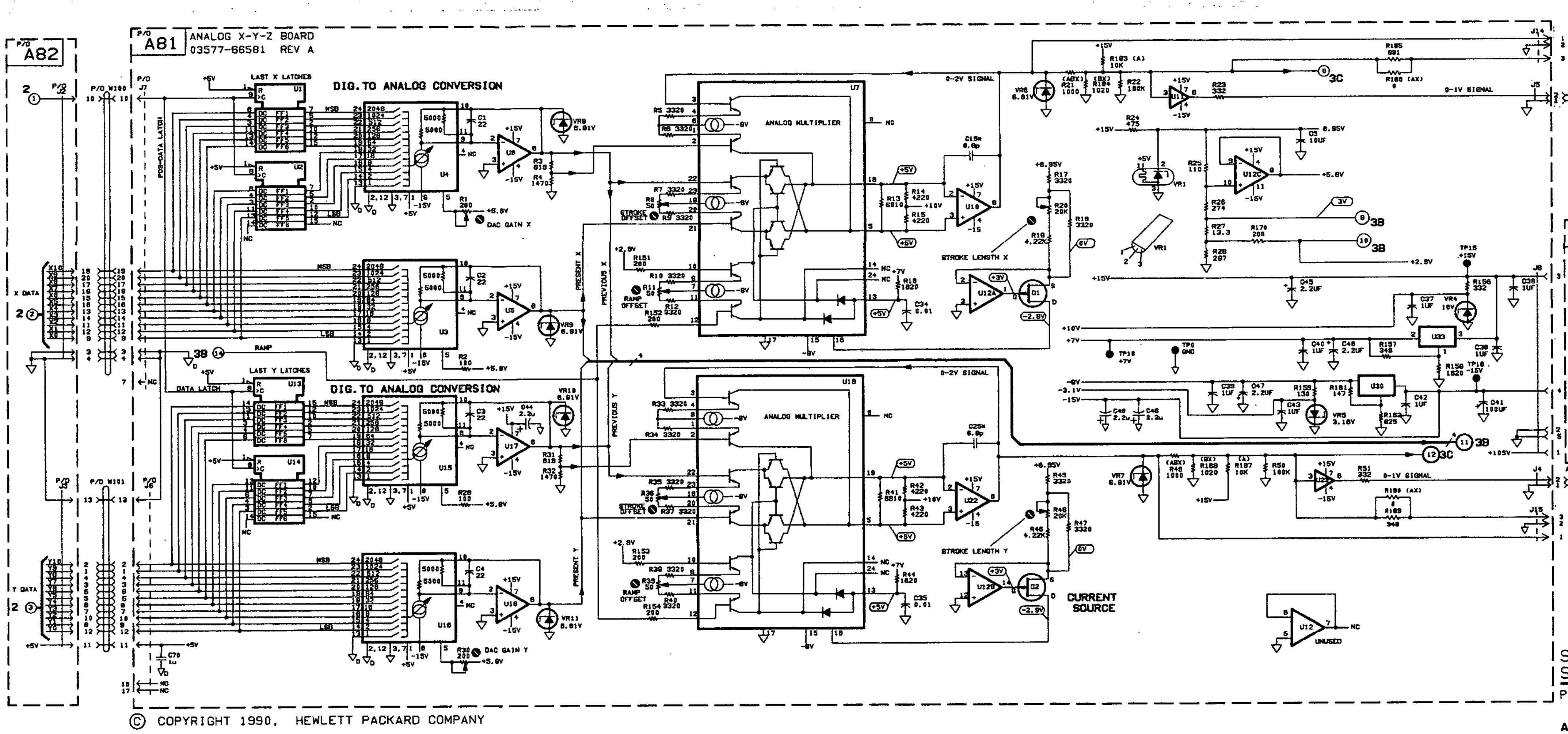
P/O 81

C12-14, C18-24, C28-33, C52-58, C58, C59
CR11-25, CR28, CR29
E1, E2
J1, J2, J10-13, J19-20
Q7-17, Q121
R23, R81-88, R90-111, R113-118, R121-146
R171-174, R177-182, R185, R187-189
TP8, TP11
U27-28, U31
VR2, VR3

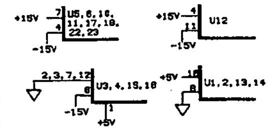
SERVICE SHEET 3C

P/O X-Y-Z AMP/STROKE GENERATOR (A81)

A81 X-Y-Z Amplifier/Stroke Generator Schematic
P/N 03577-66581
Page 3 of 5



IC DEVICE POWER CONNECTIONS



NOTES:

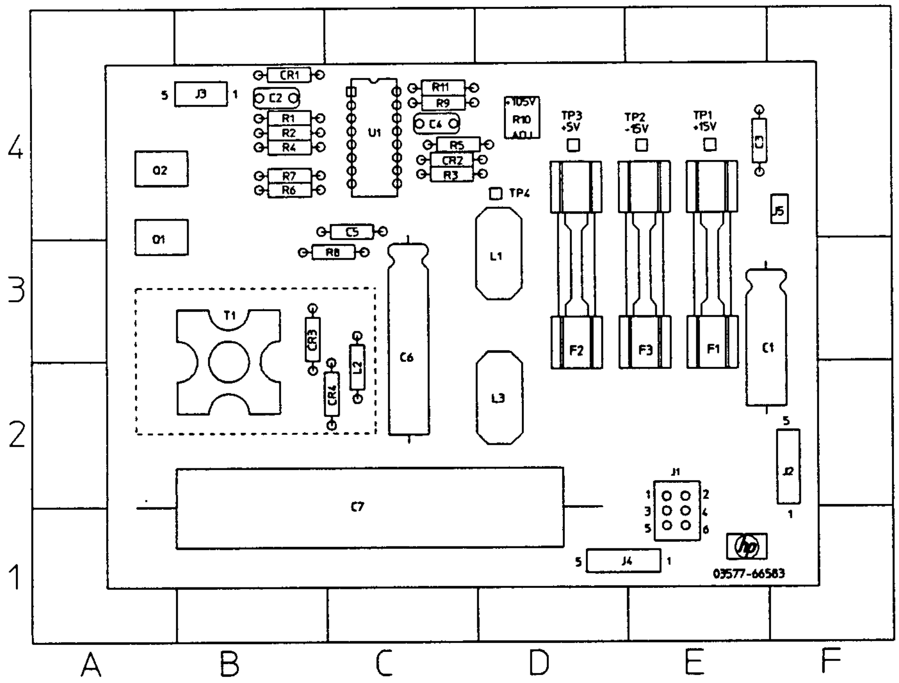
1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2V TO +5V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
5. PARTS LABELED AX, BX AND ABX ARE REMOVED ONLY FOR SPECIAL OPTIONS. R183 AND R187 LABELED (A) ARE REMOVED IN STANDARD DISPLAYS.

PARTS ON THIS SCHEMATIC		
P/O A81	A82	CHASSIS
C1-5, 15, 25, C34-48, 70 J4, 5, 8, 9, 14, 15 P/O J8, P/O J7 Q1, 2 R1-51, 151-154, 158-159, 181, 182 170, 183-189 U1-7, 10-19, 22, U23, 30, 33 VR1, 4-11	P/O J2 P/O J3	P/O W100 P/O W104
	A83	
	P/O W102	

SERVICE SHEET 3A

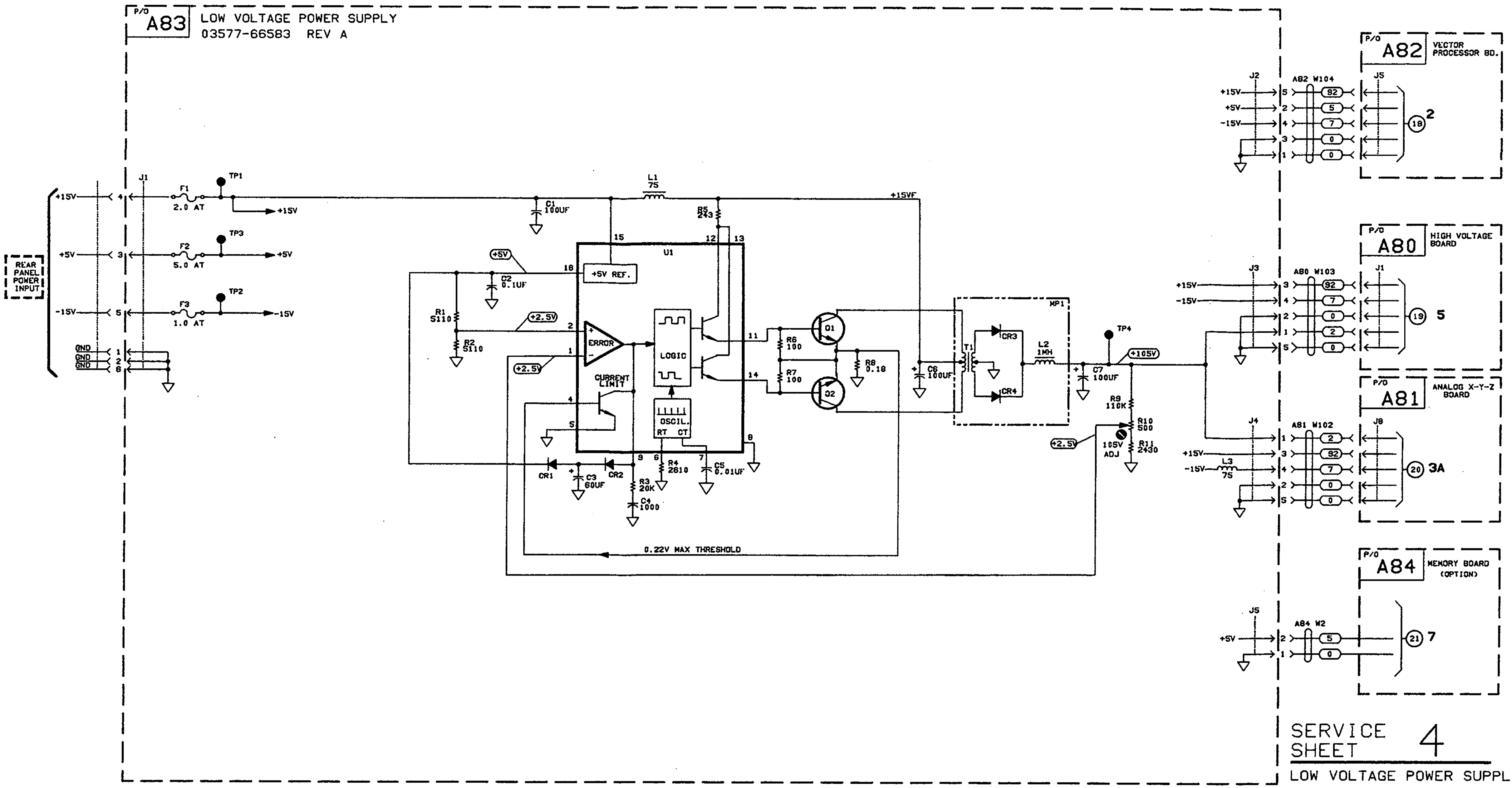
P/O X-Y-Z AMP/STROKE GENERATOR (A81)

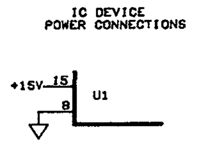
A81 X-Y-Z Amplifier/Stroke Generator Schematic
P/N 03577-66581
Page 5 of 5



Ref Desig	Grid Loc	Ref Desig	Grid Loc
C1	E-3	L3	D-2
C2	B-4	Q1	A-3
C3	E-4	Q2	A-4
C4	C-4	R1	B-4
C5	C-3	R2	B-4
C6	C-3	R3	C-4
C7	C-2	R4	B-4
CR1	B-4	R5	C-4
CR2	C-4	R6	B-4
CR3	B-2	R7	B-4
CR4	B-2	R8	B-3
F1	E-2	R9	C-4
F2	D-2	R10	D-4
F3	E-2	R11	C-4
J1	E-2	T1	B-3
J2	E-2	TP1	E-4
J3	B-4	TP2	E-4
J4	D-1	TP3	D-4
J5	F-4	TP4	D-4
L1	D-3	U1	C-4
L2	C-3		

A83 Low Voltage Power Supply Component Locator
P/N 03577-66583 Rev A
Page 1 of 2





NOTES:

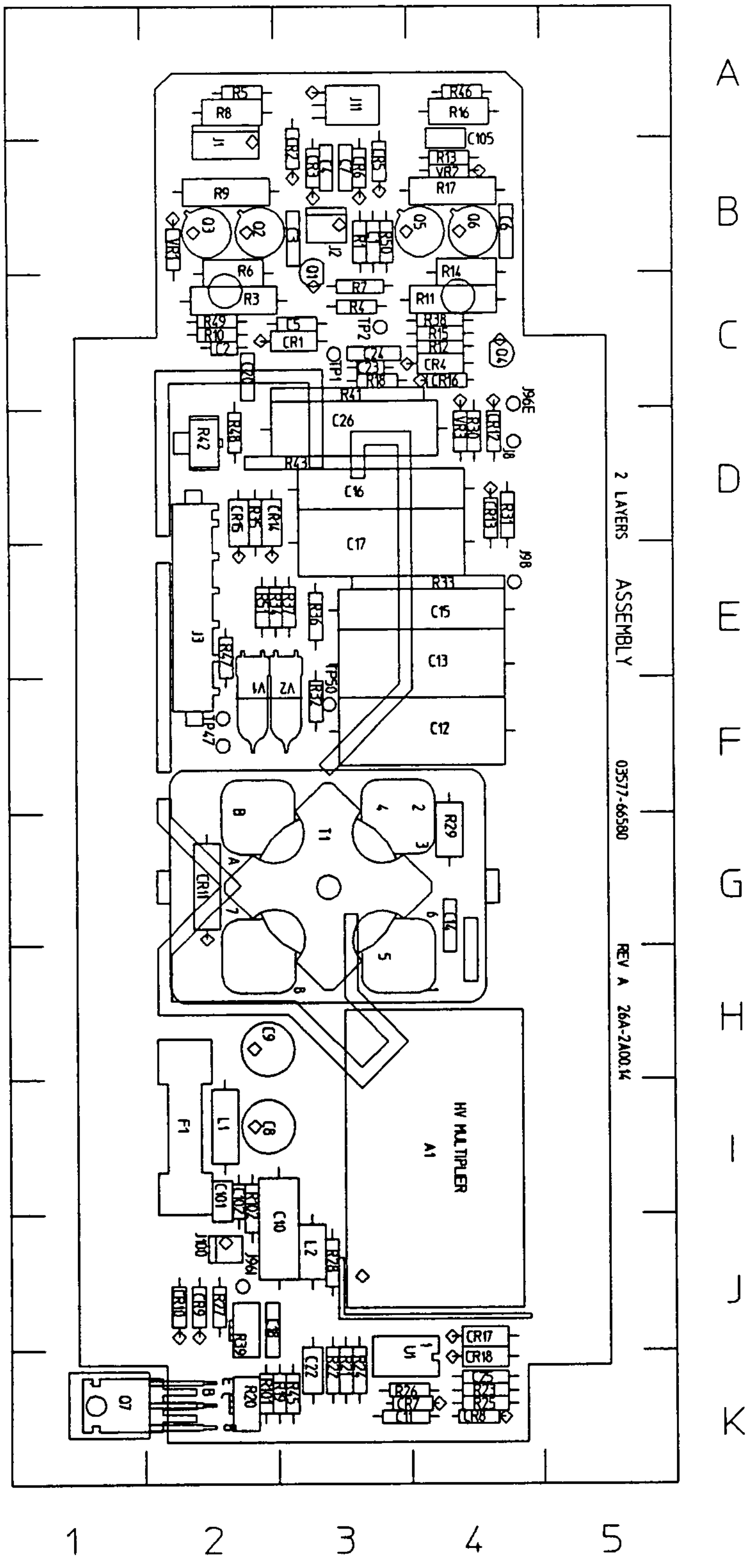
1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2V TO +5V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC		
A83	P/O A80	P/O A82
C1-7 U1 CR1-4 F1-3 J1-5 L1-3 Q1,2 R1-11 T1 TP1-4	J1	J5
	P/O A81	CHASSIS
	J8	W2 W102 W103 W104

SERVICE SHEET 4

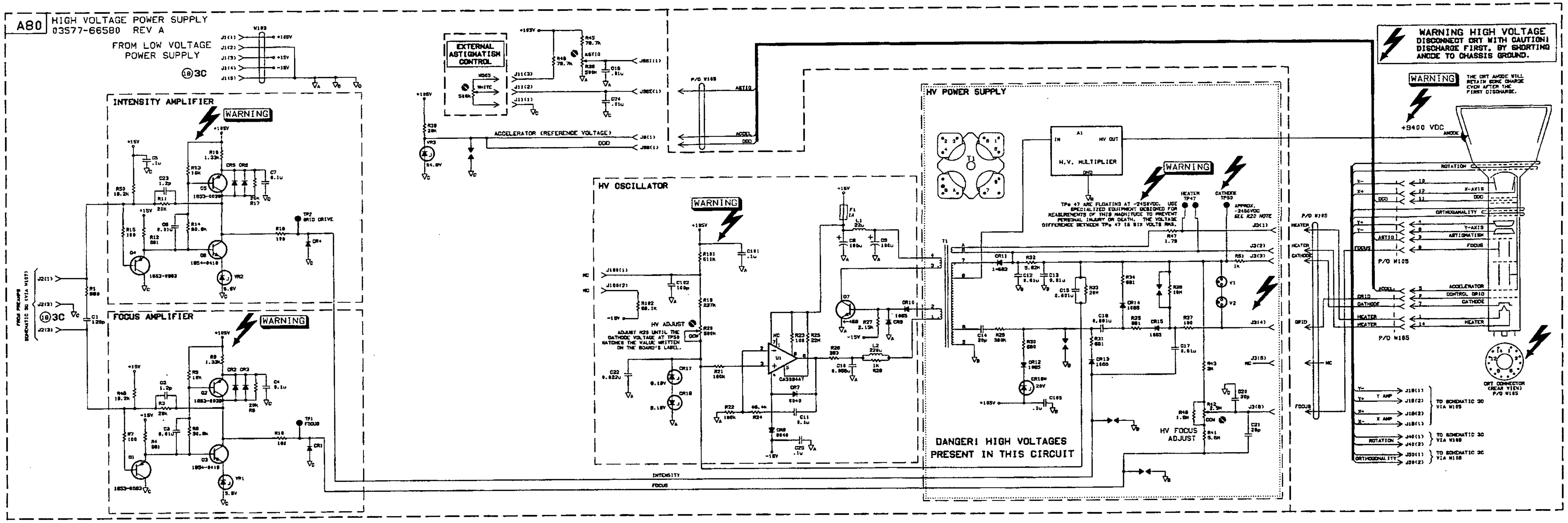
LOW VOLTAGE POWER SUPPLY (A83)

A83 Low Voltage Power Supply Schematic
P/N 03577-66583
Page 2 of 2



Ref Desig	Grid Loc	Ref Desig	Grid Loc
A1	J-3	R5	A-2
C1	B-3	R6	C-2
C2	C-2	R7	C-3
C3	B-3	R8	A-2
C4	B-3	R9	B-2
C5	C-3	R10	C-2
C6	B-4	R11	C-4
C7	B-3	R12	C-4
C8	I-2	R13	B-4
C9	H-2	R14	C-4
C10	I-2	R15	C-4
C11	K-3	R16	A-4
C12	F-4	R17	B-4
C13	E-4	R18	C-3
C14	G-4	R19	K-2
C15	E-4	R20	K-2
C16	D-3	R21	J-3
C17	E-4	R22	J-3
C18	J-2	R23	K-4
C19	J-2	R24	J-3
C20	C-2	R25	K-4
C21	C-2	R26	K-3
C22	J-3	R27	J-2
C23	C-4	R28	J-3
C24	C-3	R29	F-4
C25	K-4	R30	D-4
C26	D-4	R31	D-4
CR1	B-2	R32	F-2
CR2	B-3	R33	E-4
CR3	B-3	R34	E-2
CR4	B-4	R35	D-2
CR5	B-3	R36	E-2
CR6	B-3	R37	D-2
CR7	K-3	R38	C-4
CR8	K-4	R39	J-2
CR9	J-2	R40	J-2
CR10	J-2	R41	C-3
CR11	H-2	R42	D-2
CR12	D-4	R43	D-2
CR13	D-4	R45	K-3
CR14	E-2	R46	A-4
CR15	E-2	R47	F-2

A80 High Voltage Power Supply Component Locator
P/N 03577-66580 Rev A
Page 1 of 2


A80
HIGH VOLTAGE POWER SUPPLY
03577-66580 REV A
FROM LOW VOLTAGE POWER SUPPLY
⑩3C
INTENSITY AMPLIFIER
WARNING
FOCUS AMPLIFIER
WARNING
FROM PREAMPS SCHEMATIC 3C (VIA W107)
TP2 GRID DRIVE
TP1 FOCUS
EXTERNAL ASTIGMATISM CONTROL
ACCELERATOR (REFERENCE VOLTAGE)
DDD
P/O W105
ASTIG
ACCEL
HV OSCILLATOR
WARNING
HV ADJUST
ADJUST R20 UNTIL THE CATHODE VOLTAGE AT TP50 MATCHES THE VALUE WRITTEN ON THE BOARD'S LABEL.
INTENSITY
FOCUS
HV POWER SUPPLY
A1
IN
HV OUT
H.V. MULTIPLIER
GND
WARNING
TPs 47 ARE FLOATING AT -2450VDC. USE SPECIALIZED EQUIPMENT DESIGNED FOR MEASUREMENTS OF THIS MAGNITUDE TO PREVENT PERSONAL INJURY OR DEATH. THE VOLTAGE DIFFERENCE BETWEEN TPs 47 IS SIX VOLTS RMS.
HEATER TP47
CATHODE TP50
APPROX. -2450VDC SEE R22 NOTE
HV FOCUS ADJUST
DANGER! HIGH VOLTAGES PRESENT IN THIS CIRCUIT
WARNING HIGH VOLTAGE
DISCONNECT CRT WITH CAUTION! DISCHARGE FIRST, BY SHORTING ANODE TO CHASSIS GROUND.
WARNING
THE CRT ANODE WILL RETAIN SOME CHARGE EVEN AFTER THE FIRST DISCHARGE.
+9400 VDC
ANODE
ROTATION
X-AXIS
DDD
ORTHOGONALITY
Y-AXIS
ASTIGMATISM
FOCUS
ACCELERATOR
CONTROL GRID
CATHODE
HEATER
P/O W105
CRT CONNECTOR (REAR VIEW) P/O W105
Y AMP
X AMP
TO SCHEMATIC 3D VIA W105
TO SCHEMATIC 3C VIA W108
TO SCHEMATIC 3C VIA W108

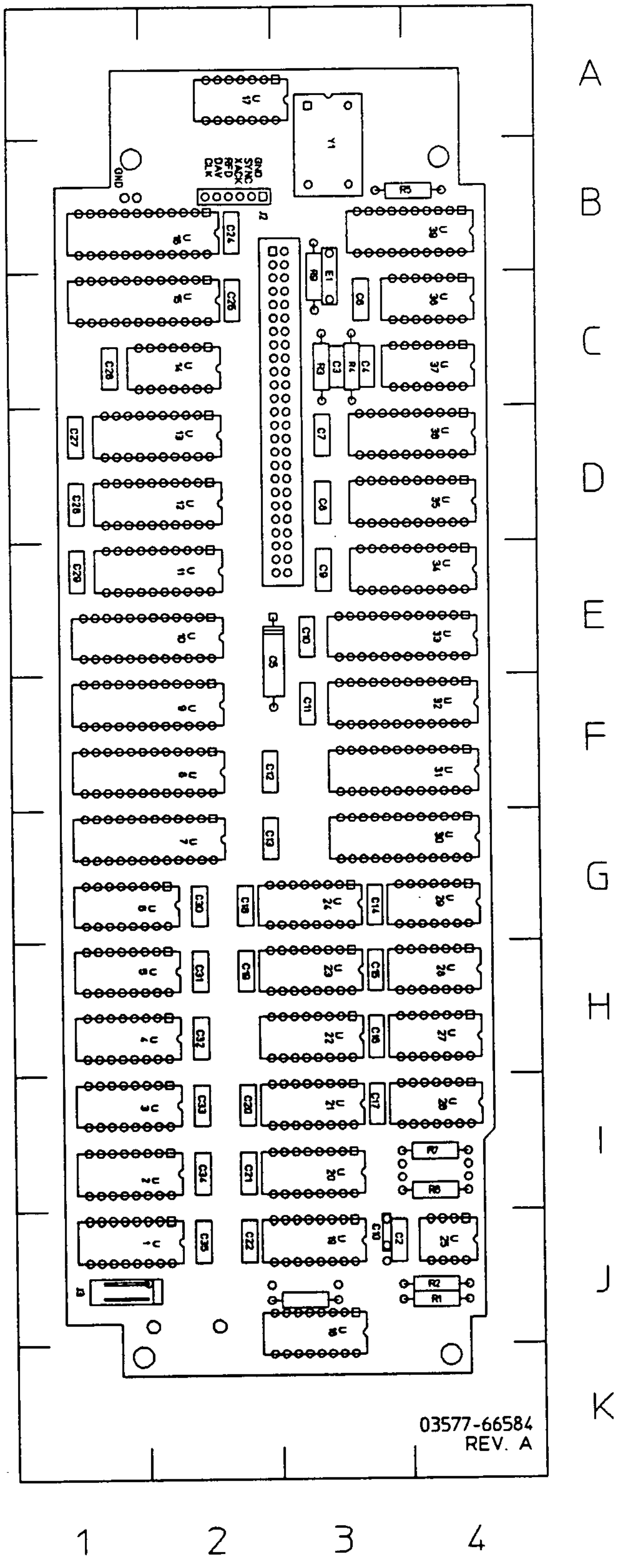
PARTS ON SCHEMATIC

A1
C1-10,C20,C22-28,C101,C102,C105
CR1-18
F1
J1-3,J100
L1,L2
Q1-7
R1,R3-39,R41-43,R45-51,R101,R102
T1
TP1,TP2,TP47,TP50,TP60
U1
V1,V2
VR1-3

SERVICE SHEET 5

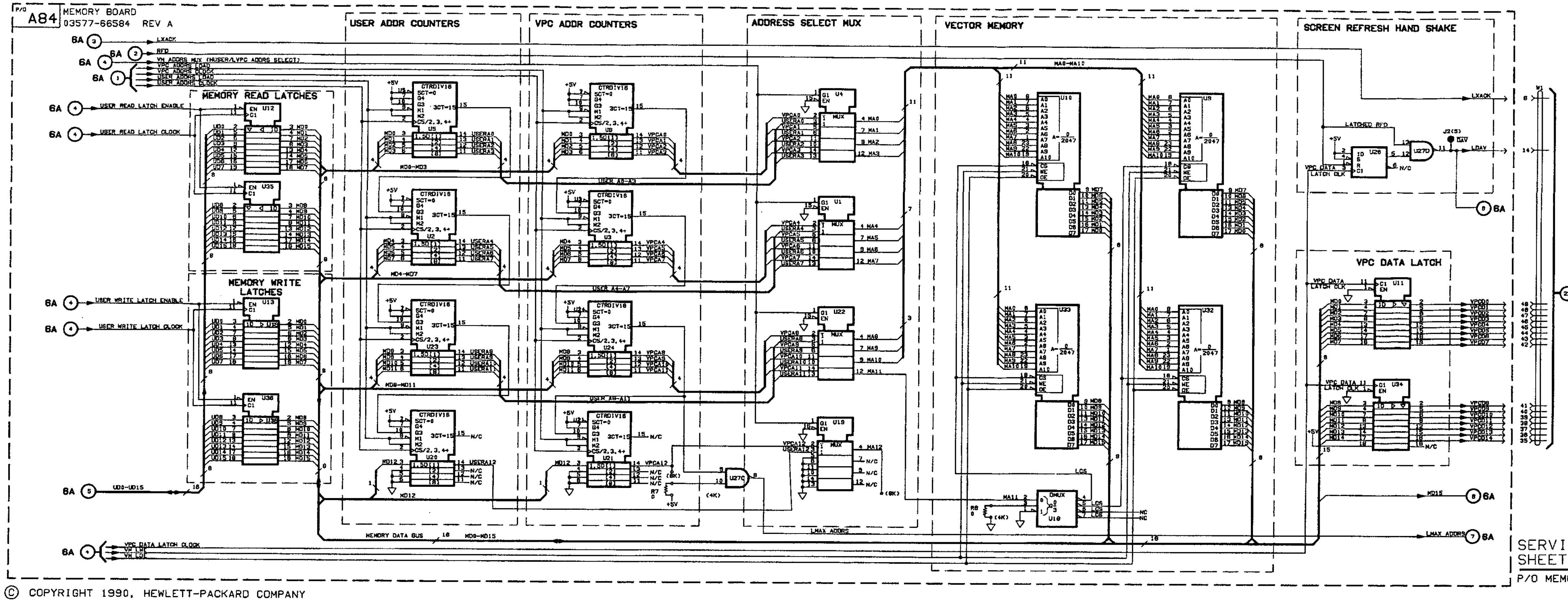
HIGH VOLTAGE POWER SUPPLY (A80)

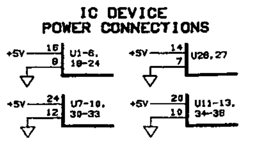
A80 High Voltage Power Supply Schematic
P/N 03577-66580
Page 2 of 2



Ref Desig	Grid Loc	Ref Desig	Grid Loc
C1	I-3	R7	H-4
C2	I-3	R8	J-3
C4	C-3	R9	C-3
C5	E-2	U1	I-1
C6	C-3	U2	H-1
C7	D-3	U3	H-1
C8	D-3	U4	I-1
C9	E-3	U5	I-1
C10	E-3	U6	G-1
C11	F-3	U9	F-2
C12	F-2	U10	E-2
C13	G-2	U11	E-2
C14	G-3	U12	D-2
C15	H-3	U13	D-2
C16	H-3	U14	C-2
C17	H-3	U15	C-2
C18	G-2	U16	B-2
C19	H-2	U17	A-2
C20	H-2	U18	J-3
C21	I-2	U19	I-3
C22	I-2	U20	H-3
C23	J-2	U21	H-3
C24	B-2	U22	I-3
C25	C-2	U23	I-3
C26	D-1	U24	G-3
C27	D-1	U25	I-4
C28	D-1	U26	H-4
C29	E-1	U27	I-4
C30	G-2	U28	I-4
C31	H-2	U29	G-4
C32	H-2	U30	G-4
C33	H-2	U31	F-4
C34	I-2	U32	F-4
C35	I-2	U33	E-4
E1	C-3	U34	E-4
J1	B-2	U35	D-4
J2	B-2	U36	D-4
J3	J-1	U37	C-4
R1	J-4	U38	C-4
R2	J-4	U39	B-4
R4	D-3	W2	B-1
R5	B-4	Y1	A-3

A84 Memory Circuit Component Locator
P/N 03577-66584 Rev A
Page 1 of 3




IC DEVICE POWER CONNECTIONS

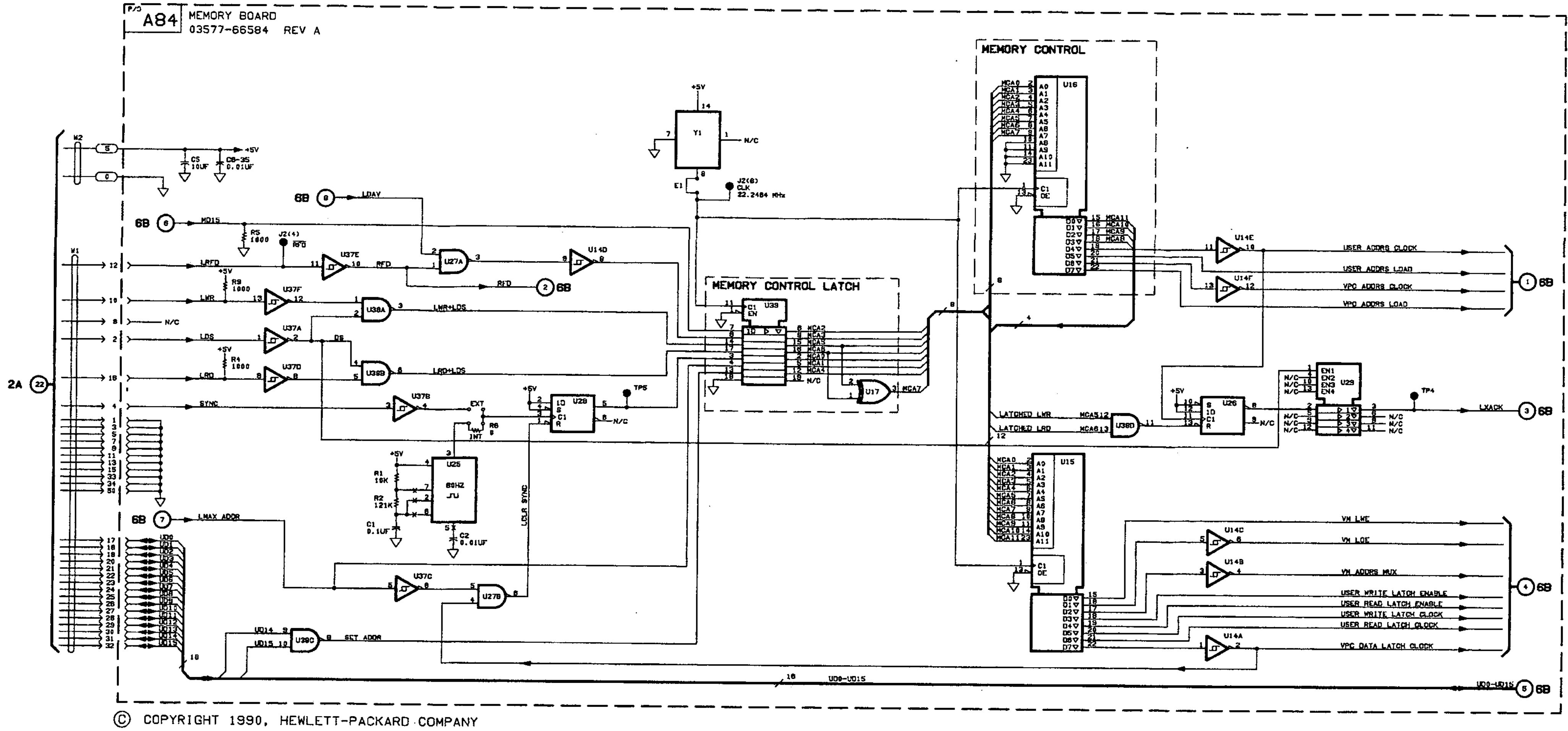
NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC	
A84	CHASSIS
R7,8 U1-13,18-24,26, 27C,27D,30-36 27C,27D,30-36	W1

SERVICE SHEET 6B

P/O MEMORY CIRCUIT (A84)



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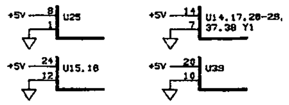
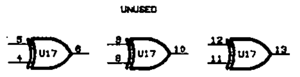
IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L



PARTS ON THIS SCHEMATIC	
A84	CHASSIS
C1,C2,C5-35 E1 R1,2,4-6,9 U14-17,25-29,37-39 W1,W2 Y1	W1 W2

SERVICE SHEET 6A

P/O MEMORY CIRCUIT (A84)

A84 Memory Circuit Schematic
P/N 03577-66584
Page 3 of 3

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PACKARD

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Service Notes

3563A-01

SERVICE NOTE

SUPERSEDES None

3563A Control Systems Analyzer

Serial Numbers: 2927A00100 to 3001A00276

Modification prevents instrument lock-up when using synthesis table.

Performed By: HP-Qualified Personnel

Parts Required:

HP P/N	Description
03563-84403	ROM Upgrade Kit

"Program ROM Dead" is displayed on the screen if more zeros than poles are entered in a synthesis table.

1. Press the line switch on.
2. Determine the firmware revision installed in the instrument by pressing the following keys:

<SPCL FCTN>
[SERVIC TEST]
[TEST RESULT]
[FAULT LOG]

DATE 01 April 1990

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

MODIFICATION RECOMMENDED

ACTION CATEGORY:	☐ IMMEDIATELY ☐ ON SPECIFIED FAILURE ■ AGREEABLE TIME	STANDARDS: LABOR: 0.5 Hours		
LOCATION CATEGORY:	☐ CUSTOMER INSTALLABLE ☐ ON-SITE ■ HP LOCATION	SERVICE INVENTORY:	☐ RETURN ■ SCRAP ☐ SEE TEXT	USED PARTS: ☐ RETURN ■ SCRAP ☐ SEE TEXT
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	RESPONSIBLE ENTITY: A100		UNTIL: 01 April 1992
AUTHOR: CMG	ENTITY: A100	ADDITIONAL INFORMATION:		

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The firmware (software) revision code is listed under the "Fault Log" title.

3. Install ROM update kit 03563-84403 if the firmware revision code is <2945.

SERVICE NOTE

SUPERSEDES None

3563A Control Systems Analyzer

Serial Numbers: 0000A00000/3004A00308

Duplicate Service Note: 3562A-12

Modification extends battery life

Situation:

The life of the battery on the A2 board can be extended by a modification to the battery backup circuit. The modification reduces drain on the battery when the instrument power is off.

Solution/Action:

Use the procedure below to tie two unused NAND gate inputs to ground and to tie a third NAND gate input to ground through a 100 kohm resistor.

Parts Required:

HP P/N	Description
1200-0638	14 pin DIP socket
1820-2923	74HC10 CMOS NAND gate
0757-0465	100 kohm, 1% resistor
	Jumper wire

Continued

DATE 01 June 1990

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

MODIFICATION RECOMMENDED

ACTION CATEGORY:	☐ IMMEDIATELY ☐ ON SPECIFIED FAILURE ☒ AGREEABLE TIME	STANDARDS: LABOR:	
LOCATION CATEGORY:	☐ CUSTOMER INSTALLABLE ☐ ON-SITE ☒ HP LOCATION	SERVICE INVENTORY: ☐ RETURN ☐ SCRAP ☒ SEE TEXT	USED PARTS: ☐ RETURN ☒ SCRAP ☐ SEE TEXT
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	RESPONSIBLE ENTITY: A100	UNTIL: 01 June 1991
AUTHOR: RM	ENTITY: A100	ADDITIONAL INFORMATION:	

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Procedure:

WARNING

The following procedure requires the instrument's top cover be removed. Energy available at many points can, if contacted, result in serious personal injury.

1. Press the line switch off and remove the instrument's power cord.
2. Remove the top cover.
3. Remove the sheet metal shield covering the digital boards (A1-A9).

CAUTION

> The following steps must be performed at a static protected site to prevent static discharge damage during the handling of the PC assembly.

4. Remove the A2 board.
5. Remove A2U408.
6. Solder the 14 pin DIP socket into place at A2U408.
7. Solder the jumper wire on the circuit side of the A2 board to connect pins 2 and 13 of A2U408 to pin 1 (ground) of A2U408.
8. On the circuit side of the A2 board, connect the 100 kohm resistor between pins 9 and 7 (ground) of A2U408.
9. Insert the NAND gate (1820-2923) into the socket at A2U408.
10. Replace the A2 board, the sheet metal shield, and the top cover.

SERVICE NOTE

SUPERSEDES: None

HP 3563A Control Systems Analyzer

Serial Numbers: 0000A00000/3004A01137

New 03562-61608 cable may cause A1 assembly short.

Duplicate service notes: 3562A-13

Parts Required:

HP Part Number	Description	Qty
0890-0060	Teflon Tubing	6mm

Situation:

The 03562-61608 cable is now being made using a SMB connector with a square body. The corners can touch the leads of capacitor C420 and resistor R508 on the 03562-66501 (A1) PC assembly causing a short.

When replacing an older cable (one with a round connector body) with the new cable, tubing should be placed on the leads of C420 and R508 that are towards J10 (one piece per component). A1 assemblies with a date code of 3508 or greater already have this tubing in place.

DATE: May 1995

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:		
INFORMATION ONLY		
AUTHOR: DLC	ENTITY: A100	ADDITIONAL INFORMATION:

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Solution/Action:

The following steps assume that the 03562-66501 (A1) PC assembly has already been removed for cable replacement.

CAUTION

The following steps must be performed at a static protected workstation to prevent static discharge to the PC assembly.

1. Unsolder the leads of C420 and R508 that are adjacent to J10.
2. Slip a 3mm piece of tubing over each component lead.
3. Resolder the leads of C420 and R508.

The 03562-66501 (A1) assembly is now ready for installation and use with the new 03562-61608 cable.

SERVICE NOTE

SUPERSEDES: None

3563A Control Systems Analyzer

Serial Numbers: 0000A00000 / 9999Z99999

Discharged battery causes power up problems

Duplicate Service Note: 3562A-15

To Be Performed By: HP-Qualified Personnel

Parts Required:

HP P/N	Description
1420-0277	Lithium Battery
1400-0249	Tie-wrap

Situation:

Corrupt nonvolatile RAM data resulting from a normal discharge of the back-up battery on the A2 CPU/HPIB board may cause an instrument to display the error message "BAD AUTO SEQUENCE TABLE" during power up. In some cases the instrument may to fail to complete its power up tests resulting in a blank display and a 1F(hex) error code on the A2 board fault LED's.

Continued

DATE: May 1996

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION: **INFORMATION ONLY**		
AUTHOR: DLC	ENTITY: A100	ADDITIONAL INFORMATION:

PRINTED IN U.S.A.

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Solution/Action:

Use the procedure below to replace the battery (if necessary) and clear the nonvolatile RAM.

WARNING

The following procedure requires the instrument's top cover to be removed. Energy available at many points can, if contacted, result in serious personal injury.

1. Press the line switch off and remove the instrument's power cord.

2. Remove the top cover.

3. Remove the sheet metal shield covering the digital boards.

CAUTION

The following steps must be performed at a static protected site to prevent static discharge damage during the handling of the PC assembly.

4. Remove the A2 board.

5. Use a volt meter to measure the voltage of the back-up battery installed on the A2 board. Replace the battery if the measured voltage does not compare favorably with the voltage printed on the battery label.

6. Install the A2 board.

7. Verify that the instrument will power up correctly. Some instruments may still not power up. In this case place A2 J21 in the test position and turn the power on again. While the power is still on place A2 J21 back in the normal position and turn the power off. 8. Replace the sheet metal shield, and the top cover.

9. This completes the procedure.

Product Support Plan

Index# How Sent Date Sent Div#/Abr
00059 __ H/C____ 06/26/89___ A100
Prod# Type Doc H/W S/W Sector
3563A____PSP______H_______MEA
Desc.2 CHANNEL DYNAMIC SIGNAL ANALY

HEWLETT PACKARD

PRODUCT SUPPORT DIVISION • 100 Mayfield Avenue, Mountain View, California 94043, Telephone (415) 968-5600

FROM: Paul Gearhart

DATE: June 27, 1989

TO: Support Plan Distribution

SUBJECT: HP3563A Product Support Plan

CC: Claudine Govier
Lake Stevens Inst. Div.
A100

HP3563A

2 CHANNEL DYNAMIC SIGNAL ANALYZER

PRODUCT SUPPORT PLAN

Here is the Support Plan for the HP3563A 2 Channel, 100KHz Dynamic Signal Analyzer. The HP3563A has all of the features of the HP3562A plus it has Digital input and output, Z-domain curve fit and synthesis, and step, pulse, ramp, and arbitrary source types.

This product is scheduled to be first available on the September, 1989 CPL.

Please see that the information in this Support plan is distributed to all people within your control that may need to take action.

Your help in communicating the information is vital to the successful implementation of support.

Regards

Paul Gearhart

PrSD Technical Marketing

1939 1989 50

3563A

Product Support Plan

Lake Stevens Instrument Division

A100

June 23, 1989

1.0 PRODUCT INFORMATION

1.01 PRODUCT INTRODUCTION SCHEDULE

Release to sales:	July 17, 1989
Manuals available to field:	
Getting Started	October 16, 1989
Operating Manual	October 16, 1989
Programming Reference	October 16, 1989
Service Manual	October 16, 1989
Product listed on CPL:	September 1, 1989
First customer shipment:	October 16, 1989

1.1 PRODUCT DESCRIPTION

The HP3563A is a 2-channel, 100 kHz dynamic signal analyzer which offers analog and digital input and output. It can characterize signals and systems in time and frequency domains by performing waveform, spectrum and network analysis. It also contains significant analysis capabilities which help the user extract additional information from measured results.

1.2 PRODUCT FEATURES

The HP 3563A Control Systems Analyzer is a compatible superset of the HP3562A Dynamic Signal Analyzer. To the features of the HP3562A, the HP3563A adds:

* Digital input and output
* Z-domain curve fit and synthesis
* Step, pulse, ramp, and arbitrary source types

1.3 PRODUCT CONFIGURATION

The HP 3563A includes:

16-bit input probe cable (01650-61607): 3 each
16-bit input probe pod (03563-61605): 3 each
8-bit output probe cable (03563-61604): 3 each
HP 10347A Pattern Generator Probe Lead set: 3 each
Grabber (5959-0288, package of 20): 80 each (4 packages)
Pouch for cables and probes
Operating Manual (03563-90000)
  Note: The operating manual includes the installation manual (03563-90007) which includes the instrument's performance tests.
Getting Started (03563-90001)
Programming Reference (03563-90005)
Power Cord
Standard 1-year warranty

OPTIONS:

907	Front Handle Kit (HP P/N 5061-0091)
908	Rack Mount Kit (HP P/N 5061-0079)
909	Rack Mount and Front Handle Kit (HP P/N 5061-0085)
910	Extra Getting Started, Operating and Programming Manuals
914	Add Service Manual and Kit
915	DOS File Utilities (HP P/N 03563-19400 for 3.5" and HP P/N 03563-19401 for 5.25" disks)
W30	Provides 3 years of customer return service.

SOFTWARE ACCESSORIES:

None

ACCESSORIES:

HP 10346A 8-Channel TTL Tristate Buffer Pod
Termination adapter (HP P/N 01650-63201)
Transit case for one HP 3563A (HP P/N 9211-2663).

1.4 USE OF OTHER HP PRODUCTS

HP-IB: Implementation of IEEE Std 488-1978
SH1 AH1 T5 TE0 L4 LE0 SR1 RL1 PP0 DC1 DT1 C0

Disc Drives (External): Supports the 91XX, 795X, and 796X families of disc drives.

Plotters: Hewlett-Packard Graphics Language (HP-GL) digital plotters

1.5 PRODUCT SPECIFICATIONS

1.5.1 PHYSICAL SPECIFICATIONS

DIMENSIONS:

Height - 222 mm (8.75 in)
Width - 426 mm (16.75 in)
Depth - 578 mm (22.75 in)

WEIGHT:

27 kg (58 lbs) net
38 kg (84 lbs) shipping

1.5.2 ELECTRICAL SPECIFICATIONS

Power:
90 to 132 VAC, 48 to 66 Hz
198 to 264VAC, 48 to 66 Hz
450 VA maximum, 275W maximum

1.5.3 MECHANICAL SPECIFICATIONS

The instrument cools by drawing air into its back panel and blowing it out the sides. Air flow must not be restricted in these areas.

1.5.4 ENVIRONMENTAL SPECIFICATIONS

Instrument (Class B2)

Operating Temperature: 0x to 55xC
Operating Humidity: <=95% at 40xC
Storage Temperature: -40x to +75x
Altitude: <=15240 m (50,000 ft)

1.5.5 SAFETY SPECIFICATIONS

The product has been designed to meet the following safety regulations:

UL1244, Second Edition, 7/21/78 with 8/10/84 revisions
IEC 348, Second Edition, 1978
CSA 556B, 9/17/73

1.5.6 STANDARDS

The product has been designed to meet the following EMI regulation:

FTZ 526/527 (1979) (West Germany)

1.6 MARKETING DATA

1.6.1 TARGETED MARKET

Environment: The product is intended to be used in laboratory and manufacturing areas.

Application: The HP 3563A is intended to be used by engineers developing and testing next generation servo systems in office automation, aerospace, consumer electronics, communications and industrial companies as well as R&D and educational institutions.

The following table reflects the expected graphic dispersion of sales of the HP 3563A (percentage) based on sales of HP 3562A:

Sales Region	Percentage of Sales
Neely/ISC	21%
Midwest	7%
Southern	7%
Eastern	18%
U.S. - Total	53%
United Kingdom	3%
Germany	5%
Other Europe	11%
Europe - Total	19%
Canada	1%
Japan	19%
Other International	8%
ICON - Total	28%

The HP 3563A is expected to have a product life of 4 years.

1.6.2 SHIPMENT SCHEDULE

Current estimates as of June 13, 1989.

CPL date: September 1, 1989

Date of first demo shipments: October 16, 1989

Date of first customer shipments: October 16, 1989

Date of first European/ICON shipments: October 16, 1989

Expected shipment quantities for first year:

Month	U.S	Europe	ICON	Total
October, 1989	22	8	12	42
November, 1989	10	4	6	20
December, 1989	10	4	6	20
January, 1990	12	4	6	22
February, 1990	10	4	5	19
March, 1990	12	4	6	22
April, 1990	11	4	6	21
May, 1990	24	8	12	44
June, 1990	22	8	12	42
July, 1990	22	8	12	42
August, 1990	24	9	13	46
September, 1990	20	7	11	38
October, 1990	21	8	11	40

1.7 WARRANTY

The HP 3563A is covered by the standard one year bench repair instrument warranty. No parts or assemblies are excluded.

Option W30 combines factory warranty with field support to provide three (3) years of continuous warranty-like support.

2.0 SUPPORT STRATEGY

2.1 SITE PREPARATION REQUIREMENTS

There must be a power outlet for the HP 3563A to plug into.

2.2 INSTALLATION

The HP 3563A automatically runs a calibration routine at power up. Self-tests can be accessed from the self-test menu.

No revisions of the system firmware are planned for the HP 3563A. Should updates be necessary, update kits comprised of replaceable parts will be provided.

2.3 REPAIR METHOD

Repair is to be performed by bench technicians at HP service centers. Repair will be either component level or assembly replacement depending on the assembly failing. Refer to Table A for a list of the assemblies and repair method.

The service kit, HP P/N 03563-84401 is necessary for proper servicing of the HP 3563A. It contains various extender boards and adapters for testing and troubleshooting the instrument. The HP 3563A Service Kit is a superset of the HP 3562A Service Kit. If a HP 3562A Service Kit is available, only the following items need to be added to it:

(1) Test Board	HP 03563-66540
(1) Capacitive Load	HP 35660-64401
(3) 16-bit probe pod	HP 03563-61605
(3) 8-bit probe cables	HP 03563-61604
(1 pkg) Grabbers	HP 5959-0288

Estimated Annualized Failure Rate: 13%
(2,000 hrs/yr)
Estimated Mean Time To Repair: 5.0 hours
Estimated Average Repair Cost: $660
Estimated Average Parts Cost: $220

TABLE A Assembly Repair Method

Component Level Repair Assemblies:

A1 Digital Source
A2 CPU
A9 FFT
A15 Keyboard
A18 Power Supply
A30 Analog Source
A31 Trigger
A32/34 ADC
A33/35 Input
Display

Exchange Assemblies:

A4 LO
A5 Digital Filter
A7 FPP
A10 Digital I/O
A38 Memory

Replace with New Assembly:

A6 Digital Filter Controller
A14 Mother Board
A20 Digital Connector Board 1
A21 Digital Connector Board 2
A22 HP-IB Connector Board
A40 Test Board

2.4 DIAGNOSTIC DESCRIPTION

The HP 3563A has extensive, internal self-tests that are used to verify instrument operation and help the service technician quickly isolate failures.

2.5 PERFORMANCE EVALUATION STRATEGY

At introduction of the HP 3563A, the performance test, operational verification, and adjustments are to be done manually or using PRSD's HP 3562A, SCAT2 automatic performance test. Full calibration with certification is done at customer request only. Selected operational verification tests are required as a part of repair as described in the service manual.

Calibration (Manual):

Frequency:	1/year
Adjustment Time:	0.5 hours
Performance Test Time (Mature)	10 hours

Total Calibration Time (Max)	10.5 hours
Operational Verification:	1 hour

2.6 PREVENTIVE MAINTENANCE

The screen for the fan needs to be cleaned periodically.

2.7 SPECIAL TOOLS

The A40 Test Board and Common Mode Cable are recommended for the performance tests. The Capacitive Load adapter is recommended to perform the adjustments. Refer to section 3.3 for the list of recommended test equipment.

2.8 SUPPORT SERVICES

The product support life cycle for the HP 3563A is 5 years.

2.9 TECHNICAL SUPPORT REQUIREMENTS

Lake Stevens Instrument Division will maintain responsibility for hardware and software on-line support. The STARS system is to be used to enter both firmware and software (DOS utilities disk) anomalies. No subcription service will be used.

3.0 SUPPORT MATERIALS

3.1 SPECIAL MATERIALS CONSIDERATIONS

None

3.2 PARTS

3.2.1 EXCHANGE ASSEMBLIES

The quantities listed in this section are estimated as of 6/89.

Description (U.S.)(U.S.)	New P/N	EXCH P/N	New List	NEP	AFR*
A4 LO	03562-66504	03562-69504	$625	$400	0.7%
A5 DGTL FLTR	03562-66505	03562-69505	$1700	$700	0.7%
A7 FFT	03562-66507	03562-69507	$1150	$500	0.4%
A10 DGTL I/O	03563-66510	03563-69510	$TBD	$TBD	0.3%
A38 MEMORY	03563-66538	03563-69538	$TBD	$TBD	0.4%

3.2.2 NON-EXCHANGE ASSEMBLIES

The quantities listed in this section are estimated as of 6/89.

Description	P/N	New List	AFR*
A1 DGTL SCE	03562-66501	$575	0.2%
A2 CPU	03563-66502	$825	0.7%
A6 DFLTR CONT	03562-66506	$430	0.2%
A9 FFT	03562-66509	$1150	0.2%
A14 MOTHERBD	03563-66514	$TBD	0.1%
A15 KEYBD	03562-66515	$650	0.7%
A18 PWR SPLY	03562-66518	$1400	1.2%
A20 CONN BRD1	03563-66520	$TBD	0.1%
A21 CONN BRD2	03563-66521	$TBD	0.1%
A22 HP-IB	03562-66522	$240	0.1%
A30 ANLG SCE	03562-66530	$675	0.1%
A31 Trigger	03562-66531	$525	0.4%
A32/34 ADC	03562-66532	$875	0.5%
A33/35 INPUT	03562-66533	$850	0.9%
DISPLAY	03562-60100	$4100	1.9%
A40 TEST BRD	03563-66540	$TBD	0.1%

*Based on HP 3562A failure rates.

3.2.3 FIELD-REPLACEABLE COMPONENT PARTS

Here is the recommended field parts to stock to support the HP 3563A. Order one of each part.

HP Part Number	Assembly Where Used	Description
0490-1403	A33, A30	Read Relay
0699-1168	A18	R-FUSE 3.9K
1820-2923	A02	IC
1826-0109	A32	IC OPAMP
1826-0528	A32	IC OPAMP
1826-0715	A30, A32, A33	IC OPAMP
1826-1040	A18	IC VREG
1853-0036	A01, A02, A15, A18	PNP Transistor
1855-0473	A18	Power FET
2110-0003		Fuse 3 AMP
2110-0056		Fuse 6 AMP

3.3 TOOL/INVENTORY PACKAGES

RECOMMENDED TEST EQUIPMENT

The equipment required to maintain 3563A is listed in table B. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications. When substitutions are made, the user may have to modify the performance and adjustment procedures to accommodate the different operating characteristics.

Table B Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model	Use*
AC Calibrator	10 Hz to 100 kHz; 1 mV to 10V Amplitude Accuracy: +-.1% Phase Locking Capability	Fluke 5200A Alternative: HP 745A Datron 4200	P,O
Frequency Synthesizer (2)	Frequency Range: 10 Hz to 1 MHz Frequency Accuracy: 10 ppm Amplitude Range: 40 Vp-p Amplitude Accuracy: <= 0.2 dB from 1 Hz to 100 kHz 1 dB from 100 kHz to 1 MHz Dynamic Range: <= -80 dBc, 10 Hz to 100 kHz	HP 3326A Opt 002 Alternative:** (2) HP 3325A/B Opt 001 Opt 002	P,O
Digital Voltmeter	5 1/2 digit, Avg AC Voltage: 30 Hz to 100 kHz; 0.1 to 500V; +-0.1%; => 1 Mohm input impedance dc Voltage: 1V to 300V; +-0.1%	HP 3456A	P,T,F
Low Distortion Oscillator	Frequency Range: 1 Hz to 100 kHz Amplitude Range: 0.1 V to 1 Vrms Distortion: <=-80 dB (0.01%)	HP 339A Alternative: HP 3326A	P
Oscilloscope	Bandwidth: >50 MHz Two Channel; External Trigger 1 Mohm Input Impedance	HP 54100A with HP 54003A Alternative: HP 1980B HP 1740	A,T,F
Signature Analyzer	Maximum Clock: >25 MHz Clock Set up Time: <20 ns	HP 5006A Alternative: HP 5005A/B	T
Variable AC Power Supply	Voltage Range: 80 to 120 Vac Frequency Range: 60 Hz Voltage Accuracy: +-2%	***	T

Triple Output DC Power Supply	Voltage Range: +15 to -15 Vdc, 0 to +6 Vdc Power: 13 watts	HP 6235A Alternative: HP 6236A/B	T
Counter	Frequency Range: 0 Hz to 100 MHz External Frequency Standard Input: 10 MHz 10 MHz	HP 5335A Alternative: HP 5328B Opt 010	A
Logic Probe	TTL/CMOS Maximum Clock: >25 MHz	HP 545A Alternative: HP 5006A HP 5005A/B	F,T
HP 3563A Service Kit	Digital Extender Brd (HP 03562-66540) (2) Analog Extender Brd (HP 03562-66541) (2) Input/Analog Ext Brds (HP 03562-66542) Common Mode Cable (HP 03562-61620) (2) Input Extender Cable (HP 03562-61621) SMB to BNC adapter cable (HP 03585-61616) Test Board (HP 03563-66540) Capacitive Load (HP 35660-64401) (3) 16-bit input probe pod (HP 03563-61605) (3) 8-bit output probe cables (HP 03563-61604) Grabbers (HP 5959-0288, pkg of 20)	HP 03563-84401	P,A,O, F,T
Probe Cable (3)	16-bit input probe cable	HP 01650-61607	P,F,T
Probe Lead (1)	Pattern generator probe lead set	HP 10347A	P,F,T

Feedthrough Terminations			P,O
(2)	50 ohm: +-2% at dc	HP 11048C Alternative: Pomona Elect. Model 4119-50 HP 10100C	
(1)	600 ohm: +-2% at dc	HP 11095A Alternative: Pomona Elect. Model 4119-600	

Cables			
(2)	BNC to BNC: length <=30 cm	HP 8120-1838	P,O
(2)	BNC/BNC Cable 122 cm	HP 8120-1840	
(1)	BNC/Dual Banana	HP 11001-60001	
(2)	Single Banana/Single Banana	Pamona Elect. Model 2948-24-0	
Clips (2)	Alligator Clip	Pamona Elect. Model 1613-8-0	
Adapters			
(1)	BNC (m) to Dual Banana (f)	Pomona Elect. Model 1296	P,O
(2)	BNC (f) to Dual Banana (m)	HP 1251-2277	
(2)	BNC Tee (m)(f)(f)	HP 1250-0781	
(1)	BNC (f) to BNC (f)	HP 1250-0080	
Resistors (2)	Value 1 kohm Accuracy: 1% Power: 0.25W	HP 0757-0280	P
(1)	Value: 100 kohm Accuracy: 1% Power: 0.25W	HP 0757-0465	

* P - Performance Tests, A - Adjustments, O - Operational Verification, F - Fault Isolation, T - Troubleshooting

** May not meet MIL 45662A Standard

*** No specific model number is recommended, any variable AC power supply which meets the listed critical specifications may be used.

** No specific model number is recommended, any variable AC power supply which meets the listed critical specifications may be used.

3.4 MATERIAL ALLOCATION PLAN

Stocking recommendations are determined initially by service engineering. Modifications to these recommendations are made by SMO based on fluctuations in inventory levels.

3.5 KIT PACKAGING

Special packaging requirements will be included with any return to factory requests.

4.0 TRAINING

HP Bench Technicians who have attended the HP 3562A Service Training (BEI3-3562A) do not need additional training to fix the HP 3563A. The BEI3-3562A class will be given if there is sufficient demand.

5.0 DOCUMENTATION

5.1 SERVICE DOCUMENTATION

HP 3563A Service Manual:

Manual Part No: 03563-90006
Microfiche Part No: 03563-90206

The service manual provides all the information required by service personnel to test, adjust, and service the 3563A Control Systems Analyzer. The service manual is available through DMK.

5.2 USER DOCUMENTATION

Operating manual:

Manual Part No: 03563-90000 (includes Installation Guide)
Microfiche Part No: 03563-90200

Installation Guide:

Manual Part No: 03563-90007
Microfiche Part No: 03563-90207
Note: Performance Tests are included in this manual.

Getting Started:

Manual Part No: 03563-90001, includes the following:

  Getting Started:
  Manual Part No: 03563-90002
  Microfiche Part No: 03563-90202

Control System Development Using Dynamic Signal Analyzers
Manual Part No: 03563-90003
Microfiche Part No: 03563-90203

Z-Plane and Mixed-Domain Fundamentals
Manual Part No: 03563-90004
Microfiche Part No: 03563-90204

Programming Reference:

Manual Part No: 03563-90005
Microfiche Part No: 03563-90205

The user documentation will be available through DMK by first customer shipment date.